

Model Name: GA-P55-USB3

1.0

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU LGA1156-A
05	CPU LGA1156-B
06	CPU LGA1156-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	DDR III POWER CAP
10	PCH FDI,DMI,USB,PCIE,NVRAM
11	PCH DP,CLK BUFFER
12	PCH HOST,SATA,PCI
13	PCH GPIO,CTRL,AUDIO
14	PCH PWR,GND
15	PCI EXPRESS*16 SLOT
16	PCI EXPRESS*4 SLOT
17	PCI EXPRESS*1 SLOT
18	PCI SLOT 1,2,3
19	ITE 8720 LPC IO
20	COM, -PROHOT , DYNAMIC OC , LPT
21	Dual BIOS
22	ALC888
23	REAR AUDIO JACK
24	CLOCK GEN ICS9LPRS914
25	VCORE PWM ISL6334ACR
26	CPU VTT PWM ISL6322G
27	DDR 15V & VCC1 05 PCH PWM ISL6545CBZ

SHEET

TITLE

28	DISCRETE POWER
29	F PANEL , F USB , FDD
30	ATX POWER
31	Marvell 9128
32	REALTEK RTL8111D
33	TPM SLB9635TT
34	HWM,KB/MS , FAN CTRL
35	ESATA JMB362
36	IT8213-1 PATA
37	UP72022
38	TABLE LIST
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Title			
Cover Sheet			
Size	Document Number	Rev	
Custom	GA-P55-USB3	1.0	
Date:	Wednesday, December 23, 2009	Sheet	1 of 37

## GA-P55-USB3 Version: 1.0

Circuit or PCB layout change  
for next version

## Component value change history

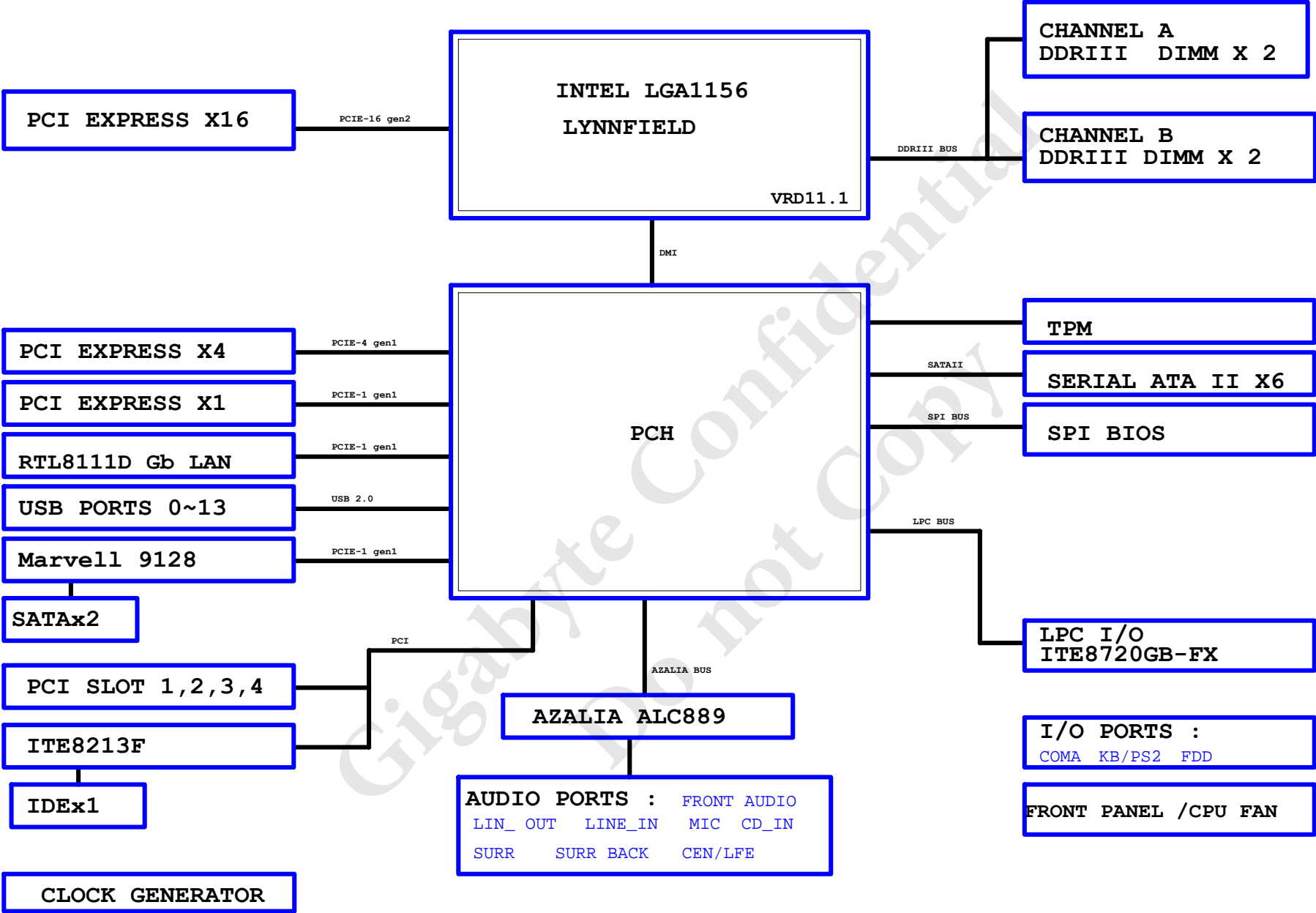
Data	Change Item	Reason
EP55A-UD3P 0.2	1. CHECK +12V SHORT PAD FOR 10mil	9. L1U1,L1U4 RTL8111D --> RTL8111C
	2. F1_1394加蓋(包材階)	10. PCB "育富"移除
	3. ADD DR86=124K/4/1 , DR88=249K/4/1	11. ONFI指定用11SM1-600078-02R
	4. U12~U15 upi6262M --> upi6267M	12. R376 2.26K/4/1 --> 2.55K/4/1
	5. DRAM_FWROK R490=1K/4/1 , R491=3K/4/1	13. 確認上哪種upi6262 10%/upi6267?
	6. REMOVE DR138=0/4 , ADD DR139,DR141=0/4	14. FB7~FB10 REMOVE
	7. RU2指定料號:10HP4-112540-11R	15. PCH BUFFER 25MHz REMOVE "X2,C93,C94,420"
	8. 排阻指定廠牌用WALSIN	16. BIOS 16M --> 32M ( FOR ONFI ONBOARD)
2009/06/10 PBOM:0.1	1.NEW MODEL: P55-UD3P-0.1	
2009/06/24 EBOM:10A	1.ADD -RSMRST PATCH CIRCUIT R866~R868,C192,C193,Q112,Q113,3UDUAL_ICH ADD 5VSB R864,R865	
	2.CHANGE Marvel9123 gpio pin,del RR39,R10,RR67,RR65,ADD RR62	
	3.CHANGE IT8275 料號,DR84 100--->0	
	4.MARVELL 9123----->JMB363	
	5.J363/J632 PATCH POWER SEQUENCE;Q50 MOS--->BJT	
2009/07/7 PBOM:10B	1.P-BOM	
2009/07/10 PBOM:10C	1.RBC53 0.1UF----->1UF	
2009/07/16 PBOM:10D	1.移除PLL電容,BC136,BC150,BC185,BC201	
2009/07/22 PBOM:10E	1.(CE2,EC32,EC37,EC38,EC23,EC36,REC3)100uf cap 6*6改成6.3*10.5mm ,因缺料	
	2.VCC3_DAC直接由VCC3經0 ohm提供	
2009/07/29 PBOM:10F	1.ADD R190 1K/4/1 FOR PCIE OVERCLOCK	
2009/08/24 EBOM:29T	1.P55-UD3P-3.0 FOR 9123/USB3.0/8213	
2009/09/9 EBOM:29A	1.CHANGE 9123;USB3.0 MP料號	
2009/10/01 EBOM:02	1.E-BOM	
2009/10/01 PBOM:10A	1.P-BOM	
P55-USB3-02	1. 包材修改	
	2. FOR H55要將CTRLCLK & CTRLDDATA移除嗎?	
P55-USB3-10A	1. ADD UE1,UE2 AZ1045	BIOS
	2. 決定R_USB30使用廠牌	1. upi6262 code改回舊版
	3. PCH要上P55/B2/B3,H55?	2. manual "ati crossfireX " remove
	4. 若是上H55 Chips,請注意KB_USB料號為11NR6-B01006-21R,U3相關零件移除,改上SR6~SR9	
	5. H55 Chips , DDCDATA/DDCCLK/DDP/CLK/DDPDATA P.U REMOVE	

DATE	Change Item	Reason
EP55A-UD3P 0.2	1. REMOVE AUDIO ESD	7. 1394 "IEC1" NET SWAP & SHORT PROTECT
	2. REMOVE CPU_VAXG	8. PIN HEATER CHECK
	3. PCH_CLK 改 SHORT PAD (0 ohm維持10pcs以下)	9. ITE8275 SYS_RST PATCH
	4. ITE8275 GPIO11,GPIO13 TO TURBO0/TURBO1	10. BC118,BC119 --> TBC29,TBC30
	5. F_PANEL UPDATE H2X10PANEL-1	11. BC5靠近M_BIOS PIN8 , BC6靠近M_BIOS PIN8
	6. ONFI 改 ON BOARD	12. U2 7474 REMOVE
EP55-UD4P 0.2	1.ONFI作塞孔	
2009/05/20 PCB:0.1	1.NEW MODEL: P55-UD3P-0.1由EP55A-UD3P-0.2修改	
2009/06/10 PCB:0.1	1.NEW MODEL: P55-UD3LP-0.1由P55-UD3P-0.1修改	
2009/06/24 PCB:1.0	1.P55-UD3P-1.0 2.修改文字面	
	3.ADD -RSMRST PATCH CIRCUIT,3UDUAL_ICH ADD 5VSB	
	4.ADD J362 POWER SEQUENCE PATCH CIRCUIT,VCC3&362_1.8V	
	5.MARVELL 9123--->J363(SPEC 變動)	
2009/07/07 PCB:1.01	1.修改文字面,加入crossFire X(PM-SALES REQUEST)	
	2.連帶更改FB5,CR64,RN21 short-wire----->電阻;ESD17 5VDUAL--->5VSB	
2009/08/21 PCB:2.9T	1.P55-UD3P-3.0 FOR 9123/USB3.0	
	2.實驗4層板及6層板(不同內層切割)	
2009/09/08 PCB:2.91	1.ADD PCIEX1 SLOT DETECT PIN FOR BIOS	
	2.EACH USB PORT USE ONE POLYFUSE	
	3.修正X16/X8 TURBO MODE 線路	
	4.調整PCICLK,USB_SEL GPIO GP40 TO GP23	
2009/09/18 PCB:1.0	1.修正X16 lane9接至switch for 9128/usb3.0 GNE2時可以斷開x16 slot端	
	2.版本改0.1,ALC888--->ALC889	
2009/09/21 PCB:0.1	1.由P55A-UD3P-1.0修正.SPEC 12相CPU為8相	
	2.DEL ESATA,NEC SWITCH	
2009/10/01 PCB:0.2	1.add NEC switch,USB 2.0 switch	
2009/10/02 PCB:1.0	1.由0.2改為1.0版	
P55-USB3-01	EVT RELEASE (From P55A-UD3 1.0)	
P55-USB3-02	1. ADD JMB363	
	2. ADD USB3.0 GEN1/GEN2 SEL SWITCH	
P55-USB3-10	1. Remove "ATI CrossFireX" Logo	

2. PE\_4\_1\_SW可預留一pull down電阻For H55 Chips
3. 文字面DES2
4. VCC2\_2,USB\_1V0在LDO加粗40mil
5. N16962199 , U2AVDD33 ICT移除
6. COMP SIDE的VIN離USB3.0的訊號太近,SOLDER SIDE也是

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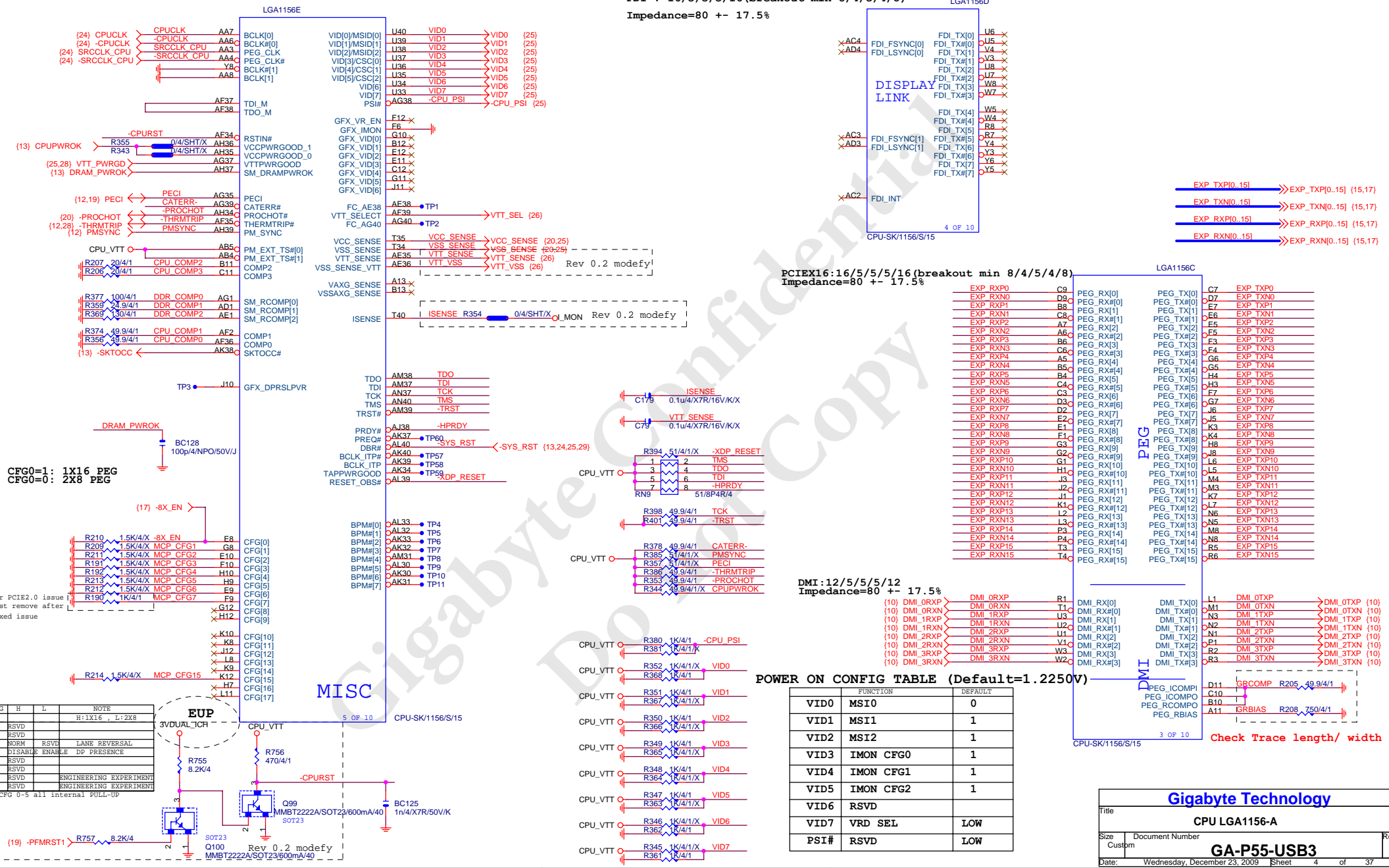
BLOCK DIAGRAM



FDI : 16/5/5/16(breakout min 8/4/5/4/8)

Impedance=80 +- 17.5%

LGA1156D



LGA1156A

MAAA0	AW18	SA_MA[0]	SA_DQS[0]	AK3	DQSA0
MAAA1	AY15	SA_MA[1]	SA_DQS[1]	CA13	-DQSA0
MAAA2	AW15	SA_MA[2]	SA_DM[0]	CA12	DMA0
MAAA3	AU15	SA_MA[3]		AH1	MDA0
MAAA4	AW14	SA_MA[4]	SA_DQ[0]	AJ4	MDA1
MAAA5	AY13	SA_MA[5]	SA_DQ[1]	AL2	MDA2
MAAA6	AV14	SA_MA[6]	SA_DQ[2]	AL1	MDA3
MAAA7	AW13	SA_MA[7]	SA_DQ[3]	AG2	MDA4
MAAA8	AU14	SA_MA[8]	SA_DQ[4]	AH2	MDA5
MAAA9	AW12	SA_MA[9]	SA_DQ[5]	AK1	MDA6
MAAA10	AT19	SA_MA[10]	SA_DQ[6]	AK2	MDA7
MAAA11	AU13	SA_MA[11]	SA_DQ[7]		
MAAA12	AW11	SA_MA[12]		AP2	DQSA1
MAAA13	AU24	SA_MA[13]	SA_DQS[11]	CA13	-DQSA1
MAAA14	AT11	SA_MA[14]	SA_DQS[11]	CA12	DMA1
MAAA15	AR10	SA_MA[15]	SA_DM[1]		
(7) -SWEA	-SWEA	AT22	SA_WE#	AN3	MDA8
(7) -SCASA	-SCASA	AU22	SA_CAS#	AN2	MDA9
(7) -SRASA	-SRASA	AT20	SA_RAS#	AR3	MDA10
(7) SBAA0	SBAA0	AV20	SA_DQ[10]	AR2	MDA12
(7) SBAA1	SBAA1	AU19	SA_BS[0]	AM3	MDA11
(7) SBAA2	SBAA2	AU12	SA_BS[1]	AM2	MDA13
			SA_BS[2]	AP1	MDA14
				AR4	MDA15
(7) -CSA0	-CSA0	AV21	SA_CS#0		
(7) -CSA1	-CSA1	AW24	SA_CS#1	AL4	DQSA2
(7) -CSA2	-CSA2	AU21	SA_CS#2	AL3	-DQSA2
(7) -CSA3	-CSA3	AU23	SA_CS#3	AL1	DMA2
(7) CKEA0	CKEA0	AU10	SA_CKE[0]	AT4	MDA16
(7) CKEA1	CKEA1	AW10	SA_CKE[1]	AJ2	MDA17
(7) CKEA2	CKEA2	AV10	SA_CKE[2]	AW3	MDA18
(7) CKEA3	CKEA3	AY10	SA_CKE[3]	AW4	MDA19
				AT3	MDA20
MODT_A0	AV23	SA_ODT[0]		AT1	MDA21
MODT_A1	AV24	SA_ODT[1]		AV2	MDA22
MODT_A2	AW23	SA_ODT[2]		AV4	MDA23
MODT_A3	AY24	SA_ODT[3]			
(7) DCLKA0	DCLKA0	AR22	SA_CK[0]	AY6	DQSA3
(7) -DCLKA0	-DCLKA0	AR21	SA_CK#0	AW6	-DQSA3
(7) DCLKA1	DCLKA1	AP18	SA_CK[1]	AW6	DMA3
(7) -DCLKA1	-DCLKA1	AN18	SA_CK#1		
(7) DCLKA2	DCLKA2	AN21	SA_CK[2]	AW5	MDA24
(7) -DCLKA2	-DCLKA2	AP21	SA_CK#2	AY5	MDA25
(7) DCLKA3	DCLKA3	AP19	SA_CK[3]	AJ8	MDA26
(7) -DCLKA3	-DCLKA3	AN19	SA_CK#3	AY8	MDA27
(7,8) -DDR3_RST	-DDR3_RST	AV8	SM_DRAMRST#	AJ5	MDA28
				AV7	MDA30
				AW7	MDA31
AK22	SA_CS#4	SA_DQS[4]	AR28	DQSA4	
AM22	SA_CS#5	SA_DQS#4	CA129	-DQSA4	
AL23	SA_CS#6	SA_DM[4]	AN29	DMA4	
AK23	SA_CS#7				
AL10	SA_DQS[8]		AN27	MDA32	
AM10	SA_DQS#8		AT28	MDA33	
AP10	SA_ECC_CB[0]		AP28	MDA34	
AN10	SA_ECC_CB[1]		AP30	MDA35	
AR11	SA_ECC_CB[2]		AN26	MDA36	
AP11	SA_ECC_CB[3]		AR27	MDA37	
AK9	SA_ECC_CB[4]		AR29	MDA38	
AL9	SA_ECC_CB[5]		AN30	MDA39	
AK11	SA_ECC_CB[6]				
AM11	SA_ECC_CB[7]				
			AV32	DQSA5	
			CAW32	-DQSA5	
			AW31	DMA5	
			AL30	MDA40	
			AL31	MDA41	
			AV33	MDA42	
			AL34	MDA43	
			AV30	MDA44	
			AW30	MDA45	
			AL33	MDA46	
			AW33	MDA47	
			AW36	DQSA6	
			CAV35	-DQSA6	
			AL35	DMA6	
			AW35	MDA48	
			AY35	MDA49	
			AV37	MDA50	
			AL37	MDA51	
			AY34	MDA52	
			AW34	MDA53	
			AV36	MDA54	
			AW37	MDA55	
			AR38	DQSA7	
			CAAR38	-DQSA7	
			AT38	DMA7	
			AT39	MDA56	
			AT40	MDA57	
			AN38	MDA58	
			AN39	MDA59	
			AL38	MDA60	
			AP39	MDA61	
			AP38	MDA62	
			AP40	MDA63	

DDR\_A

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CPU-SK1156/S15

LGA1156B

	MAAB0	AU20	SB_MA[0]	SB_DQS[0]	AF4	DQSB0
	MAAB1	AU18	SB_MA[1]	SB_DQS[0]	AE5	-DQSB0
	MAAB2	AV18	SB_MA[2]	SB_DM[0]	AE4	DMB0
	MAAB3	AU17	SB_MA[3]			
	MAAB4	AY18	SB_MA[4]	SB_DQ[1]	AD7	MDB0
	MAAB5	AV17	SB_MA[5]	SB_DQ[2]	AD6	MDB1
	MAAB6	AW17	SB_MA[6]	SB_DQ[3]	AH8	MDB2
	MAAB7	AU16	SB_MA[7]	SB_DQ[3]	AJ8	MDB3
	MAAB8	AT17	SB_MA[8]	SB_DQ[4]	AC7	MDB4
	MAAB9	AY16	SB_MA[9]	SB_DQ[5]	AC6	MDB5
	MAAB10	AY25	SB_MA[10]	SB_DQ[6]	AF5	MDB6
	MAAB11	AW16	SB_MA[11]	SB_DQ[7]	AE6	MDB7
	MAAB12	AW15	SB_MA[12]			
	MAAB13	AW28	SB_MA[13]	SB_DQS[1]	AH6	DQSB1
	MAAB14	AY12	SB_MA[14]	SB_DQS[1]	AJ5	-DQSB1
	MAAB15	AV11	SB_MA[15]	SB_DM[1]	AH4	DMB1
(8)	-SWEB	-SWEB	SB_WE#	SB_DQ[8]	AG5	MDB8
(8)	-SCASB	-SCASB	SB_CS#0	SB_DQ[9]	AH7	MDB9
(8)	-SRASB	-SRASB	SB_CS#5	SB_DQ[9]	AK6	MDB10
			SB_CS#6	SB_DQ[11]	AL4	MDB11
(8)	SBAB0	SBAB0	SB_BS[0]	SB_DQ[12]	AG4	MDB12
(8)	SBAB1	SBAB1	SB_BS[1]	SB_DQ[13]	AJ7	MDB14
(8)	SBAB2	SBAB2	SB_BS[2]	SB_DQ[15]	AK7	MDB15
(8)	-CSB0	-CSB0	SB_CS#0		AN6	DQSB2
(8)	-CSB1	-CSB1	SB_CS#1	SB_DQS[2]	AM6	-DQSB2
(8)	-CSB2	-CSB2	SB_CS#2	SB_DQS[2]	AM7	DMB2
(8)	-CSB3	-CSB3	SB_CS#3	SB_DM[2]		
(8)	CKEB0	CKEB0	SB_CKE[0]	SB_DQ[16]	AL6	MDB16
(8)	CKEB1	CKEB1	SB_CKE[1]	SB_DQ[17]	AN5	MDB17
(8)	CKEB2	CKEB2	SB_CKE[2]	SB_DQ[18]	AP6	MDB18
(8)	CKEB3	CKEB3	SB_CKE[3]	SB_DQ[19]	AR5	MDB19
				SB_DQ[20]	AL5	MDB20
	MODT_B0	AU27		SB_DQ[21]	AN7	MDB22
	MODT_B1	AU29	SB_ODT[0]	SB_DQ[22]	AP5	MDB23
	MODT_B2	AV27	SB_ODT[1]	SB_DQ[23]		
	MODT_B3	AU28	SB_ODT[3]			
				SB_DQS[3]	AR8	DQSB3
				SB_DQS#3	AP8	-DQSB3
				SB_DM[3]	AT7	DMB3
(8)	DCLKB0	DCLKB0	SB_CK[0]	SB_DQ[24]	AT6	MDB24
(8)	-DCLKB0	-DCLKB0	SB_CK#0	SB_DQ[25]	AR7	MDB25
(8)	DCLKB1	DCLKB1	SB_CK[1]	SB_DQ[26]	AR9	MDB26
(8)	-DCLKB1	-DCLKB1	SB_CK#1	SB_DQ[27]	AM8	MDB27
(8)	DCLKB2	DCLKB2	SB_CK[2]	SB_DQ[28]	AN8	MDB28
(8)	-DCLKB2	-DCLKB2	SB_CK#2	SB_DQ[29]	AR6	MDB29
(8)	DCLKB3	DCLKB3	SB_CK[3]	SB_DQ[30]	AL6	MDB30
(8)	-DCLKB3	-DCLKB3	SB_CK#3	SB_DQ[31]	AT9	MDB31
	AM23	SA_CS#4	SA_DQS[4]	AT25	DQSB4	
	AM24	SA_CS#5	SA_DQS#4	AR24	-DQSB4	
	AL24	SA_CS#6	SA_DM[4]	AN24	DMB4	
	AK24	SA_CS#7				
				SB_DQ[32]	AN23	MDB32
				SB_DQ[33]	AP23	MDB33
				SB_DQ[34]	AR25	MDB34
				SB_DQ[35]	AR26	MDB35
				SB_DQ[36]	AT23	MDB36
				SB_DQ[37]	AP22	MDB37
				SB_DQ[38]	AP25	MDB38
				SB_DQ[39]	AT26	MDB39
				SB_DQS[5]	AP32	DQSB5
				SB_DQS#5	AR32	-DQSB5
				SB_DM[5]	AN32	DMB5
	AR12	SB_ECC_CB[0]	SB_DQ[40]	AT32	MDB40	
	AT13	SB_ECC_CB[1]	SB_DQ[41]	AP31	MDB41	
	AN15	SB_ECC_CB[2]	SB_DQ[42]	AR33	MDB42	
	AP14	SB_ECC_CB[3]	SB_DQ[43]	AM32	MDB43	
	AM12	SB_ECC_CB[4]	SB_DQ[44]	AT31	MDB44	
	AN12	SB_ECC_CB[5]	SB_DQ[45]	AR31	MDB45	
	AN14	SB_ECC_CB[6]	SB_DQ[46]	AR34	MDB46	
	AP13	SB_ECC_CB[7]	SB_DQ[47]	AT33	MDB47	
				SB_DQS[6]	AR36	DQSB6
				SB_DQS#6	AR37	-DQSB6
				SB_DM[6]	AM33	DMB6
				SB_DQ[48]	AR35	MDB48
				SB_DQ[49]	AT36	MDB49
				SB_DQ[50]	AP36	MDB51
				SB_DQ[51]	AP34	MDB52
				SB_DQ[52]	AT35	MDB53
				SB_DQ[53]	AN34	MDB54
				SB_DQ[54]	AP37	MDB55
				SB_DQ[55]		
				SB_DQS[7]	AL37	DQSB7
				SB_DQS#7	AM36	-DQSB7
				SB_DM[7]	AK35	DMB7
				SB_DQ[56]	AL35	MDB56
				SB_DQ[57]	AM35	MDB57
				SB_DQ[58]	AJ36	MDB58
				SB_DQ[59]	AJ37	MDB59
				SB_DQ[60]	AN35	MDB60
				SB_DQ[61]	AM34	MDB61
				SB_DQ[62]	AJ35	MDB62
				SB_DQ[63]	AL36	MDB63

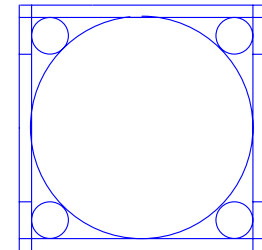
DDR\_B

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DDR\_B

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CPU-SK1156/S15

CR  
CPU RETENTION/X

Need check the new CPU ME

LGA1156



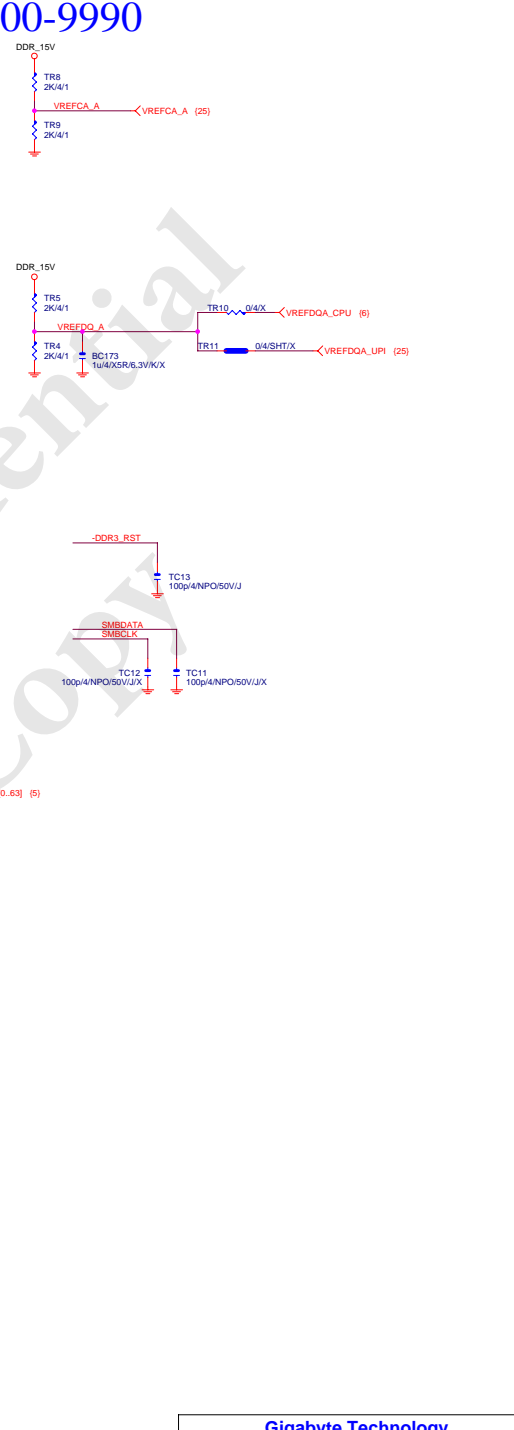
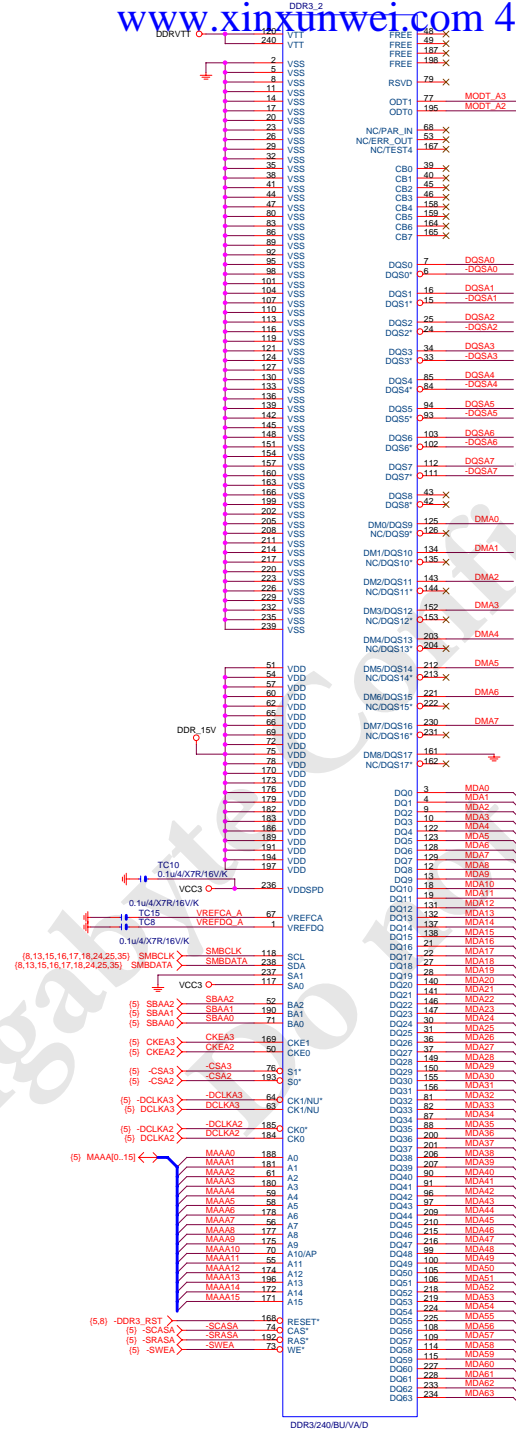
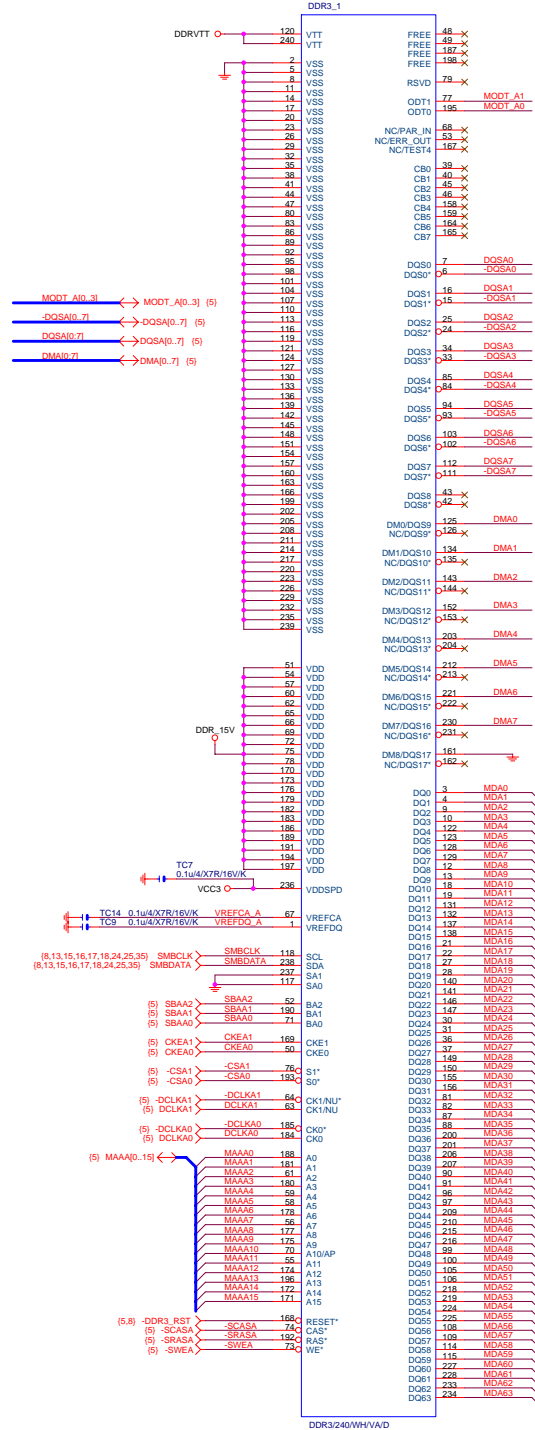
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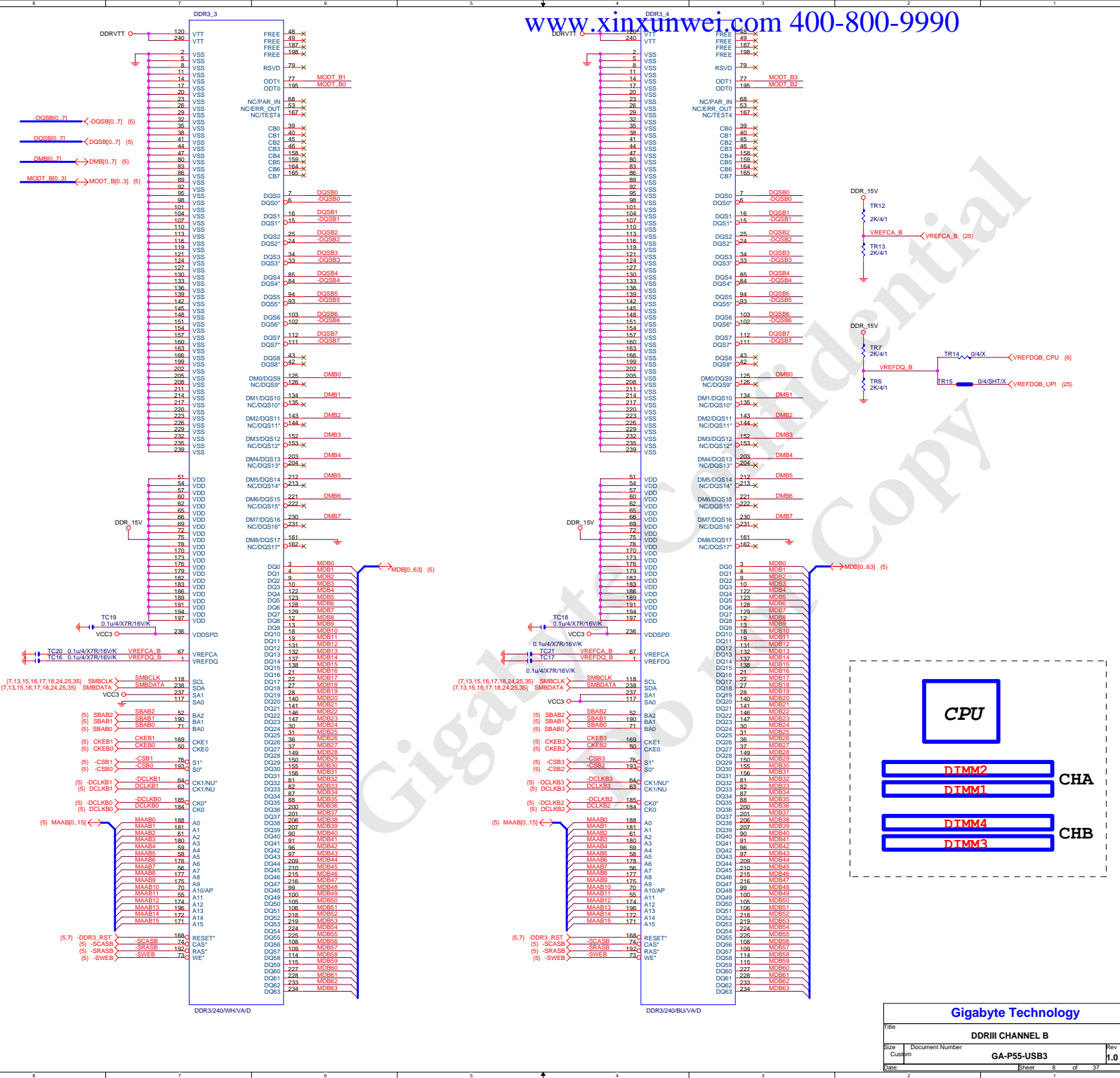
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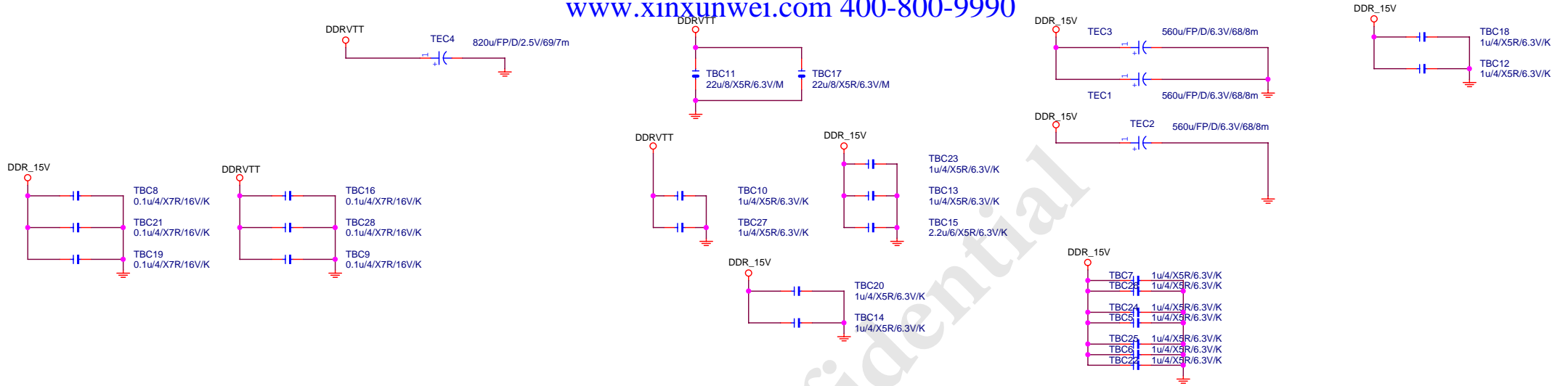












COUPON1 COUPON1 1 2 COUPON/X VCORE

COUPON2 COUPON2 1 2 COUPON/X

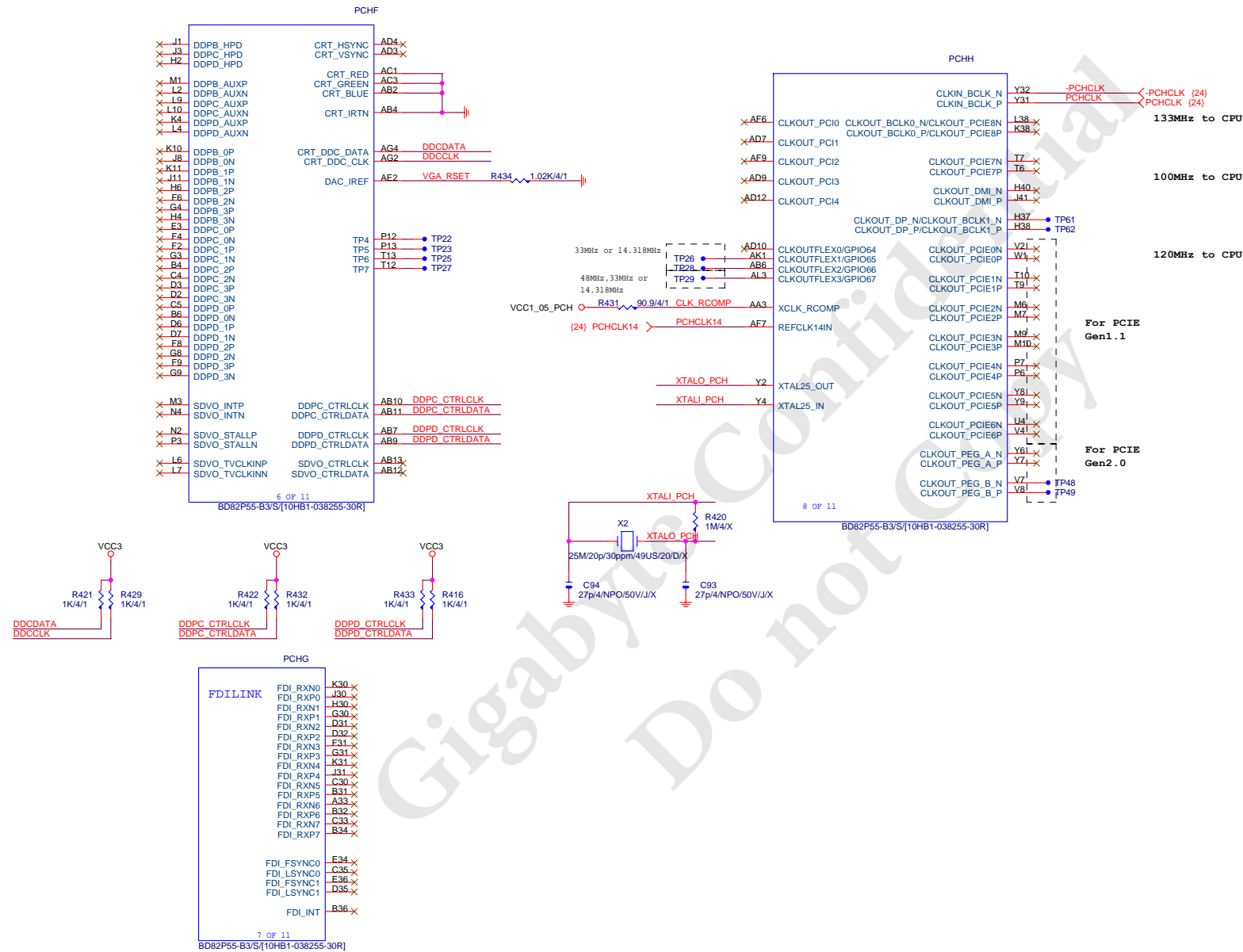
**Gigabyte Technology**

Title  
**DDRIII POWER CAP**

Size B Document Number **GA-P55-USB3** Rev 1.0

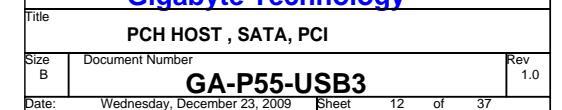
Date: Wednesday, December 23, 2009 Sheet 9 of 37





Gigabyte Technology

Title		
PCH DISPLAY ,CLK BUFFER		
Size	Document Number	Rev
Custom	GA-P55-USB3	1.0
Date:	Wednesday, December 23, 2009	Sheet 11 of 37

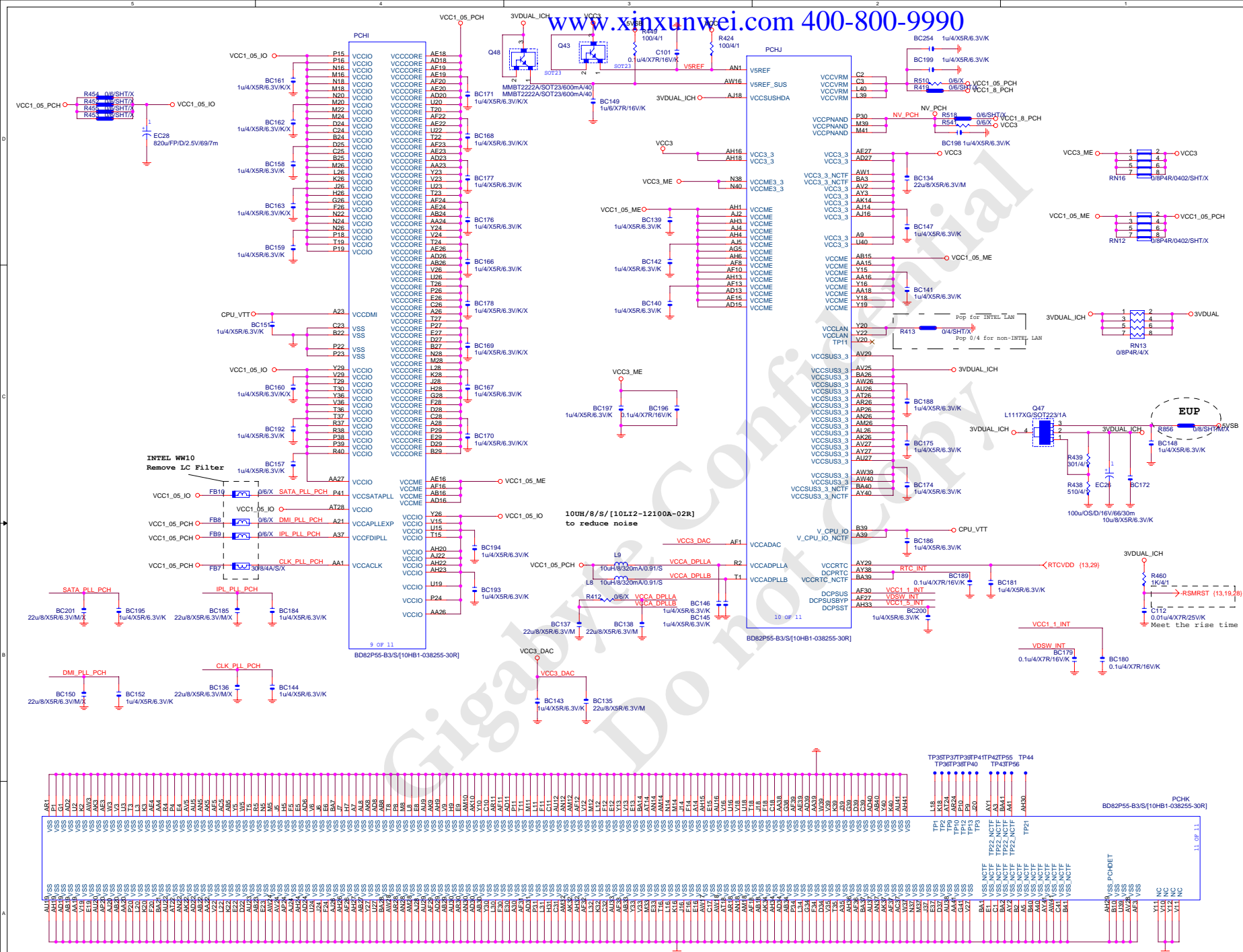




PCH GPIO CTBI AUDIO

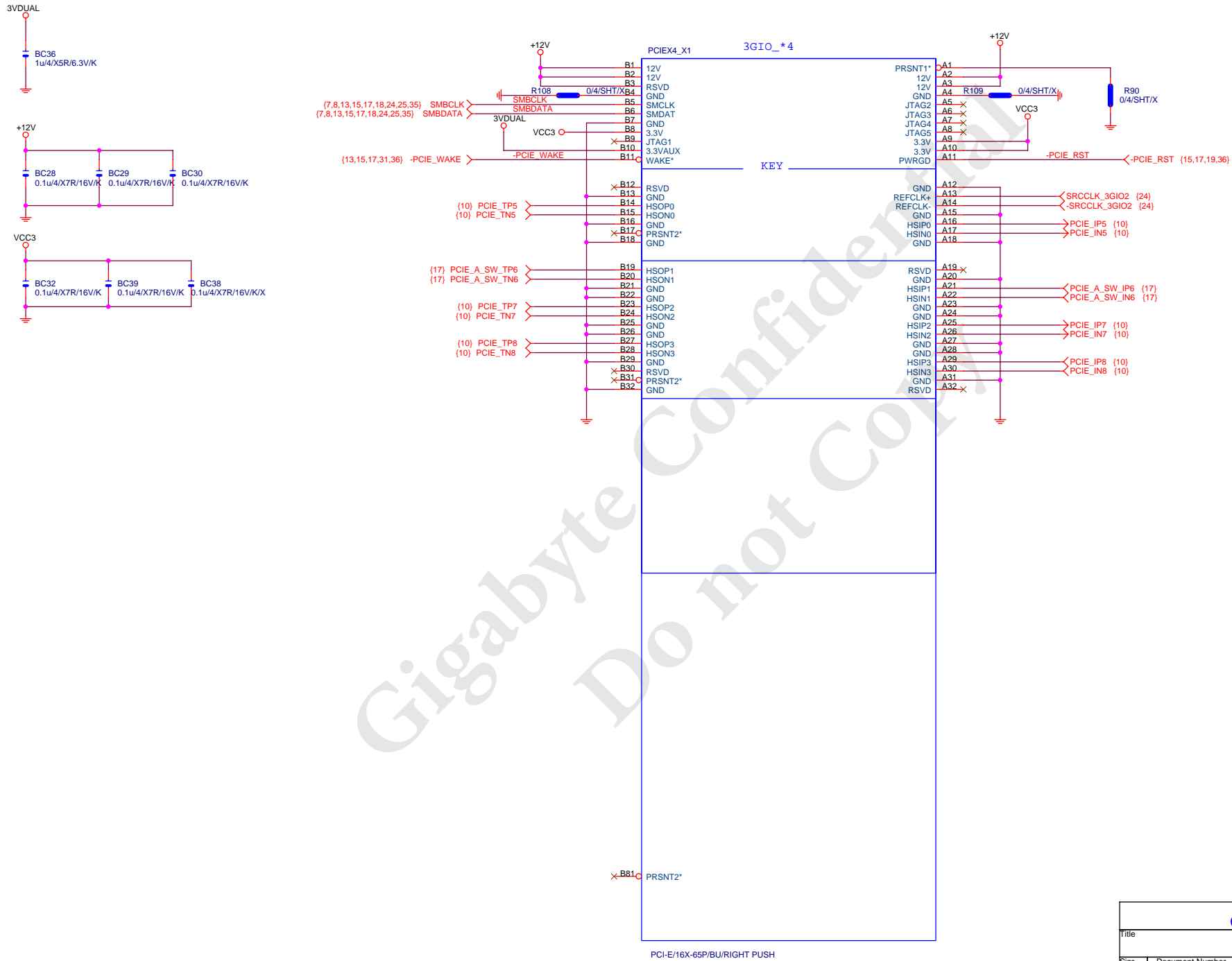
Size B	Document Number <b>GA-P55-USB3</b>	Rev 1.0
Date:	Wednesday, December 23, 2009	Sheet 13 of 37







PCI-E REV:2.0--&gt; 5GHZ

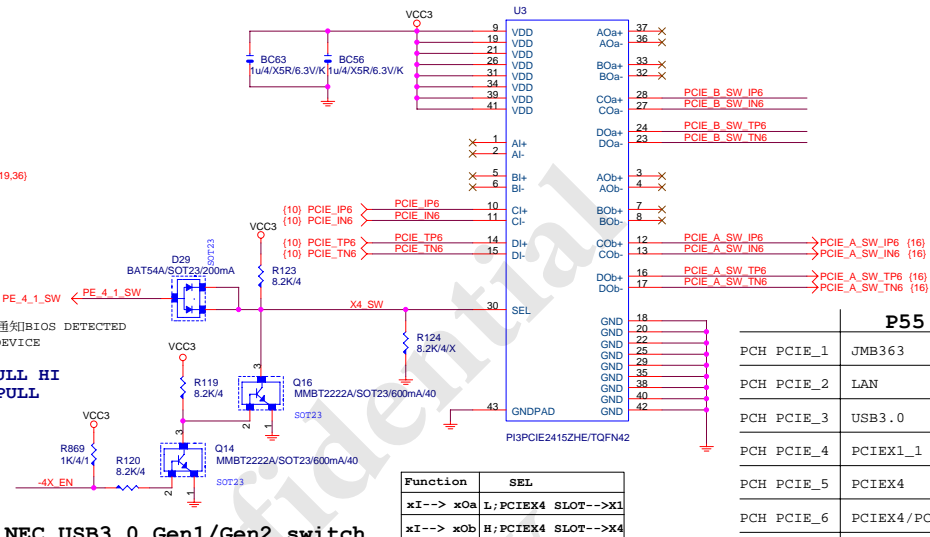
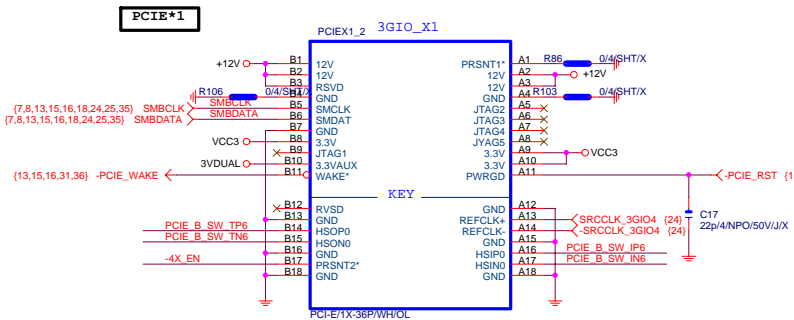
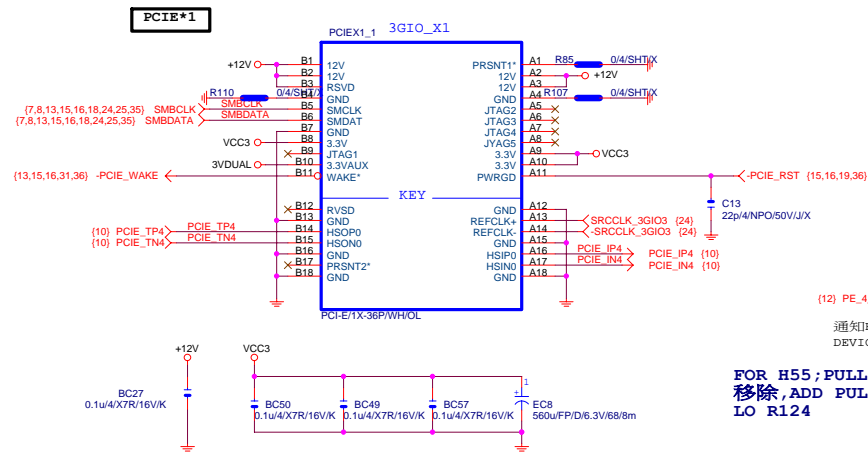


PCI-E/16X-65P/BU/RIGHT PUSH

**Gigabyte Technology**

PCI EXPRESS X 4 PORT

Title		Document Number		Rev
Size		GA-P55-USB3		1.0
Date:	Wednesday, December 23, 2009	Sheet	16	of 37



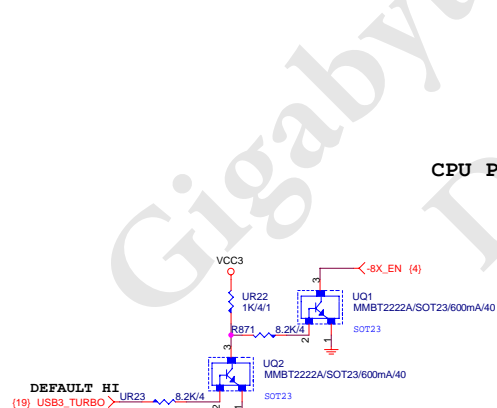
	<b>P55</b>	<b>H55</b>
PCH PCIE_1	JMB363	JMB363
PCH PCIE_2	LAN	LAN
PCH PCIE_3	USB3.0	USB3.0
PCH PCIE_4	PCIEX1_1	PCIEX1_1
PCH PCIE_5	PCIEX4	PCIEX4-->PCIEX1
PCH PCIE_6	PCIEX4/PCIEX1_2	PCIEX1_2
PCH PCIE_7	PCIEX4	N/A
PCH PCIE_8	PCIEX4	N/A

NEC USB3.0 Gen1/Gen2 switch		
	PCIE1X4->X4 : Hi PCIE1X4->X1 : Lo	PCIE1X4->X4 : Hi PCIE1X4->X1 : Lo
	X4_SW	PE_4_1_SW
PCIE1X1_2未插卡	Hi	Hi
16.19.36 PCIE1X1_2插卡	Lo	Lo

PCIE IP6 SR6 0/4/X PCIE B SW IP6  
PCIE IN6 SR7 0/4/X PCIE B SW IN6

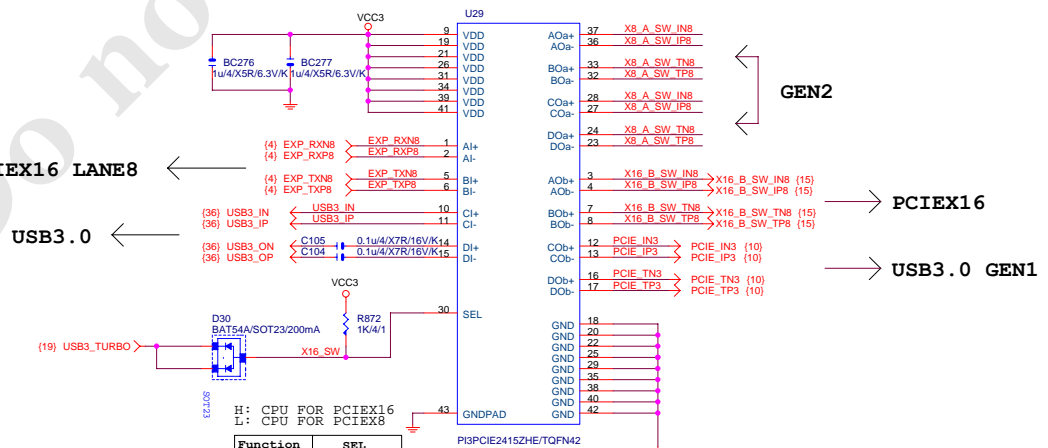
PCIE TP6 SR8 0/4/X PCIE B SW TP6  
PCIE TN6 SR9 0/4/X PCIE B SW TN6

**FOR H55 ONLY**  
**R請放在U3背面**



NEC USB3.0 Gen1/Gen2 switch

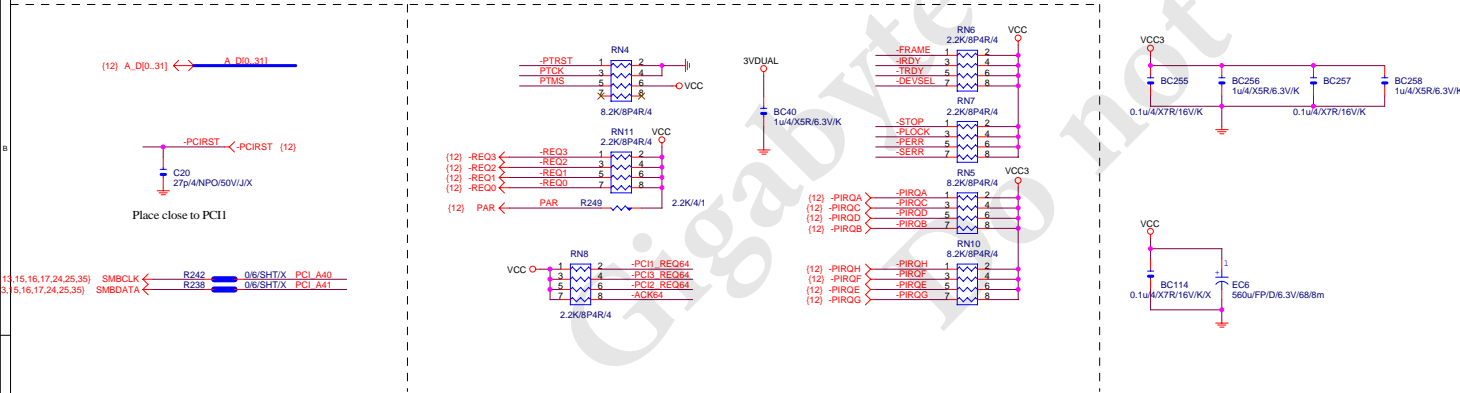
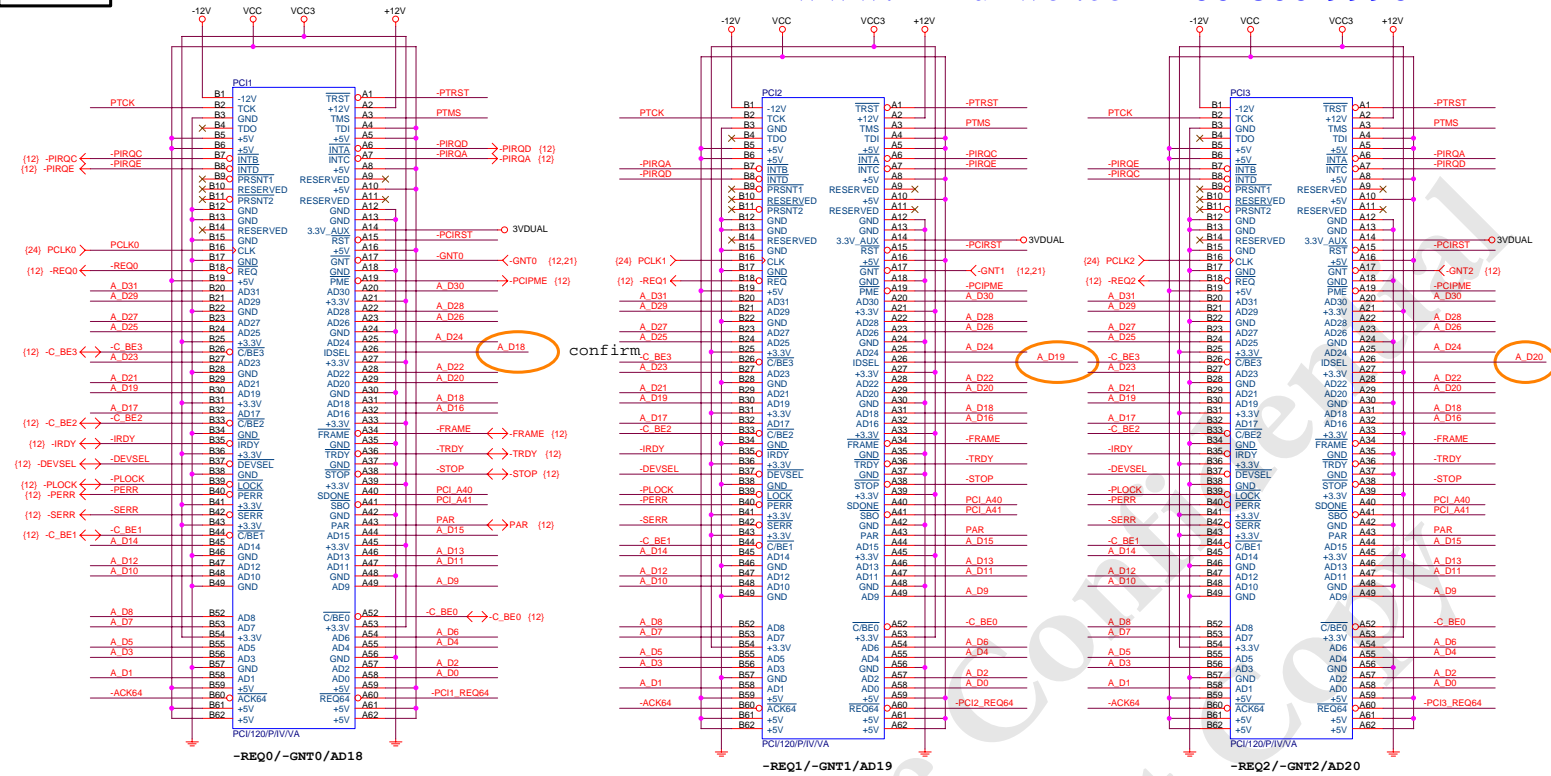
	USB3.0 Gen1 : Lo USB3.0 Gen2 : Hi	MCH X16 : Hi MCH X8 : Lo
	X16_SW	-8X_EN
USB3.0 Gen1	Hi	Hi
USB3.0 Gen2	Lo	Lo



Function	SEL
xI--> xOa	L
xI--> xOb	H

Function	SEL
USB3.0 GNE2	L
USB3.0 GNE1	H

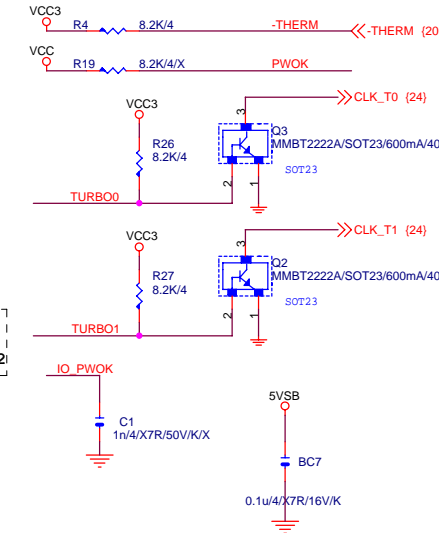
PCI1,2 SLOT



Gigabyte Technology

File	PCI SLOT 1, 2, 3		Rev
Size	Document Number	GA-P55-USB3	1.0
Date	Wednesday, December 23, 2009	Sheet	18 of 37

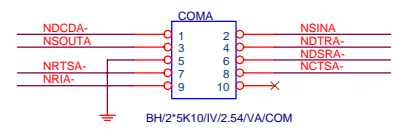
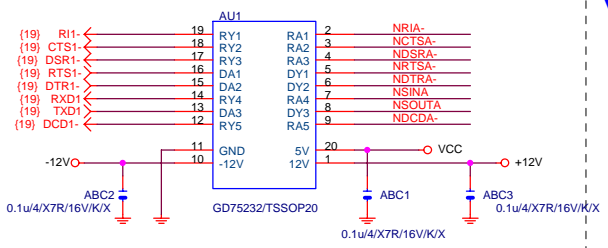




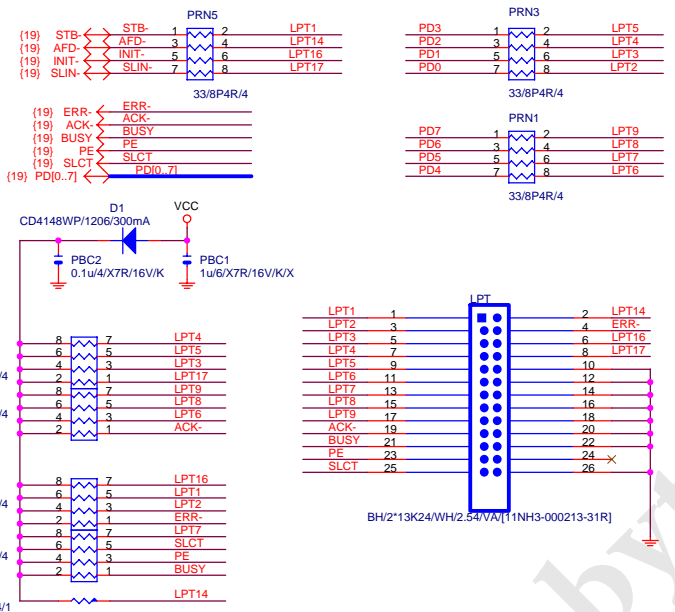
JP2	1	Disable VID/SVID output pins
	0	Enable VIDO0-7 output pins
JP3	1	SPI-Flash Disable
	0	SPI-Flash Enable
JP4	1	k8 power sequency function is Disable
	0	k8 power sequency function is Enable
JP5	1	Disable WDT reset PWROK
	0	Enable WDT reset PWROK
JP6	1	Parallel VID output
	0	Serial VID output
JP7	1	Enable Dual BIOS Function
	0	Disable Dual BIOS Function

Title			
ITE 8720 LPC IO			
Size B	Document Number		Rev 1.0
GA-P55-USB3			
Date:	Wednesday, December 23, 2009	Sheet	19 of 37

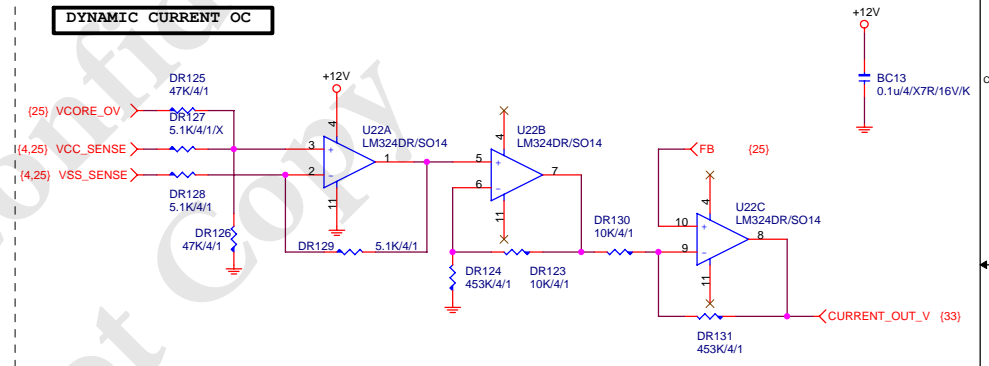
COMA



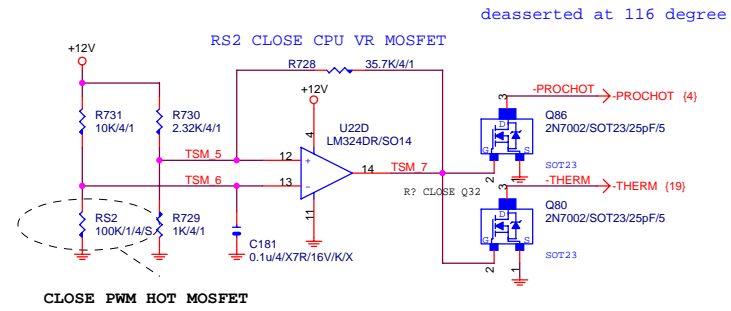
LPT PORT



DYNAMIC CURRENT OC



-PROHOT



Gigabyte Technology			
Title			
COM & PROHOT/Dynamic O.C.			
Size	Document Number	Rev	
Custom		1.0	
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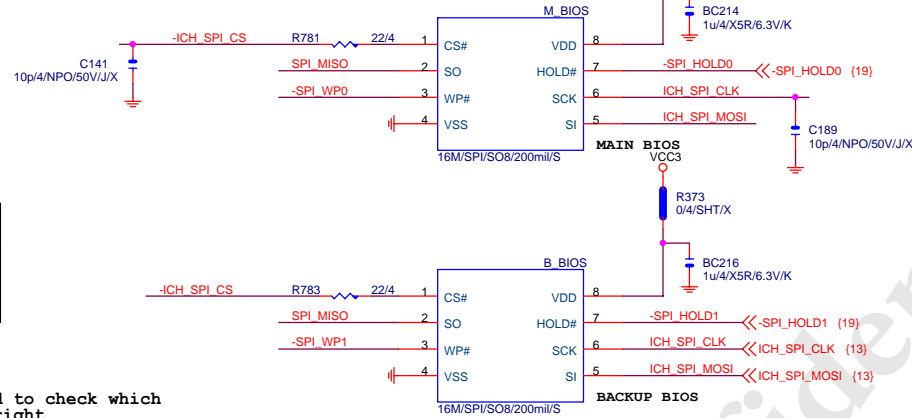
VCC3  
BC215  
0.1u/4/X7R/16V/K

C141  
10p/4/NPO/50V/J/X

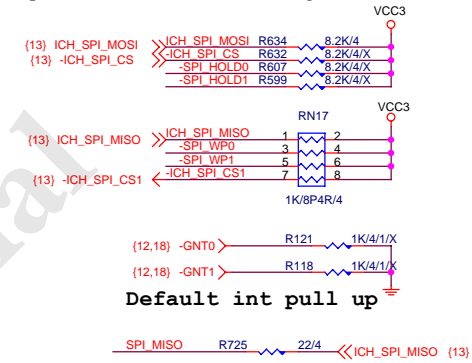
BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating  
0 means PD 1K

IC8SO-SOCKET need to check which  
is right



MOSI pull up to enable iTPM , floating to disable



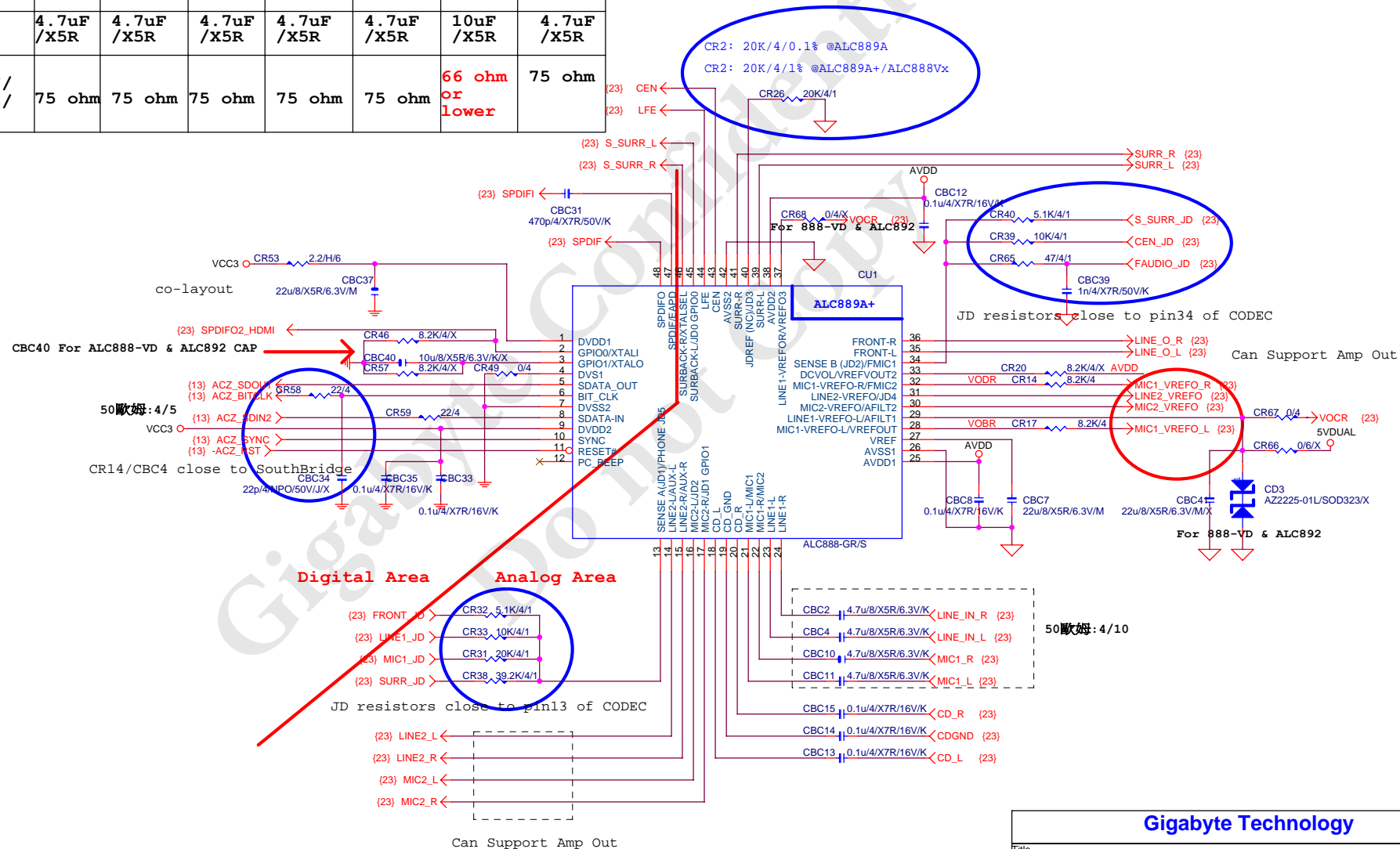
Default int pull up

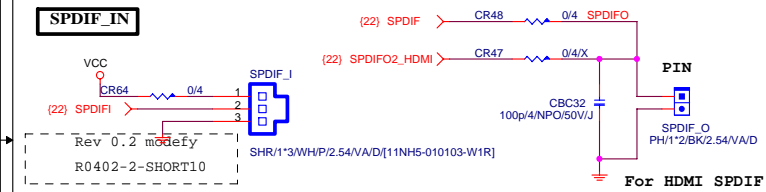
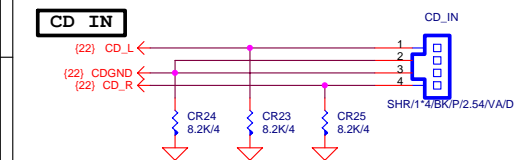
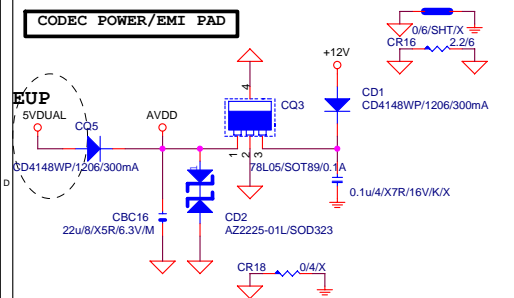


Gigabyte Technology

Title		BIOS	
Size	Document Number	GA-P55-USB3	
Custom		Rev 1.0	
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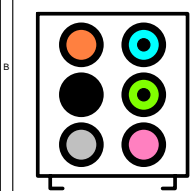
	ALC883	ALC888-VA	ALC888B	ALC888-VD	ALC892	ALC889	ALC889A
CR46	X	X	X	X	X	X	O
CR57	X	X	X	X	X	X	O
CR49	O	O	X	X	X	O	O
CBC40	X	X	X	10uF/X5R	10uF/X5R	X	X
CR20	O	X	X	X	X	X	X
CR26	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/1%	20K/0.1%
CR47	X	X	X	X	O	O	X
CR48	O	O	O	O	X	X	O
CBC2/CBC4/CBC5/ CBC6/CBC10/CBC11	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR1/CR3/CR10/CR12/ CR15/CR19/CR56/CR27/ CR55/CR37/CR28/CR34/ CR6/CR9/CR51/CR61	75 ohm	75 ohm	75 ohm	75 ohm	75 ohm	66 ohm or lower	75 ohm



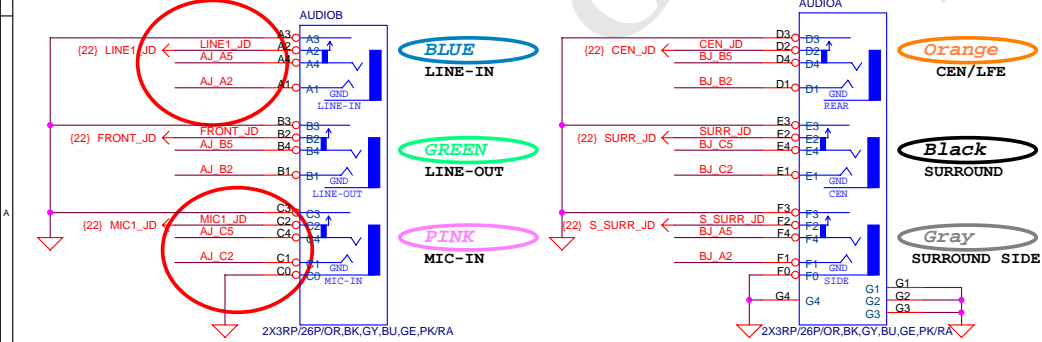


**AZALIA JACK**

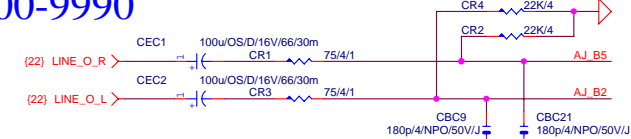
BTX AZALIA CONNECTOR



11NR6-403007-21R



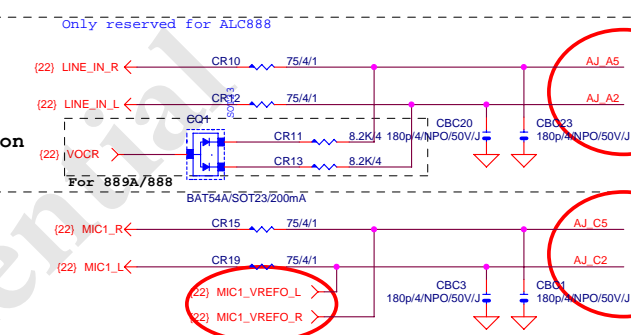
**LINE-OUT**



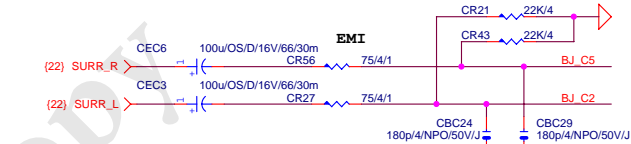
**LINE-IN**

Verify MIC function  
in LINE-in

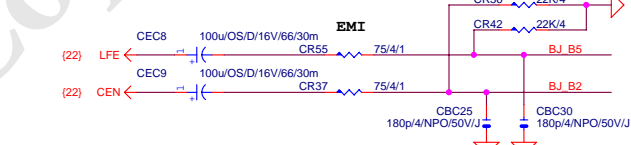
**MIC-IN**



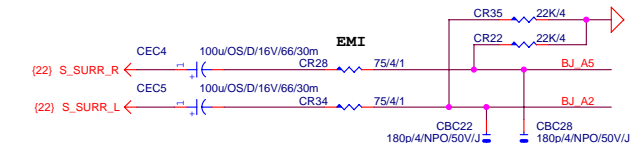
**SURROUND**



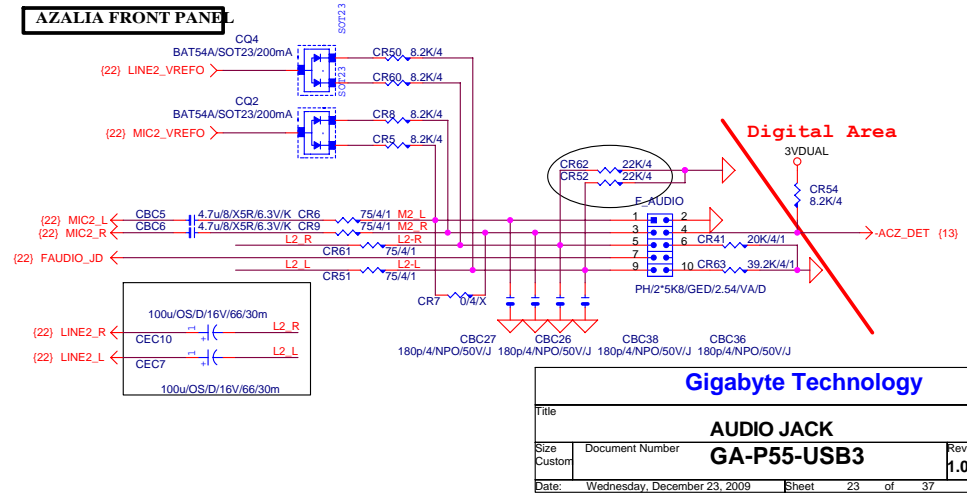
**CEN/LFE**



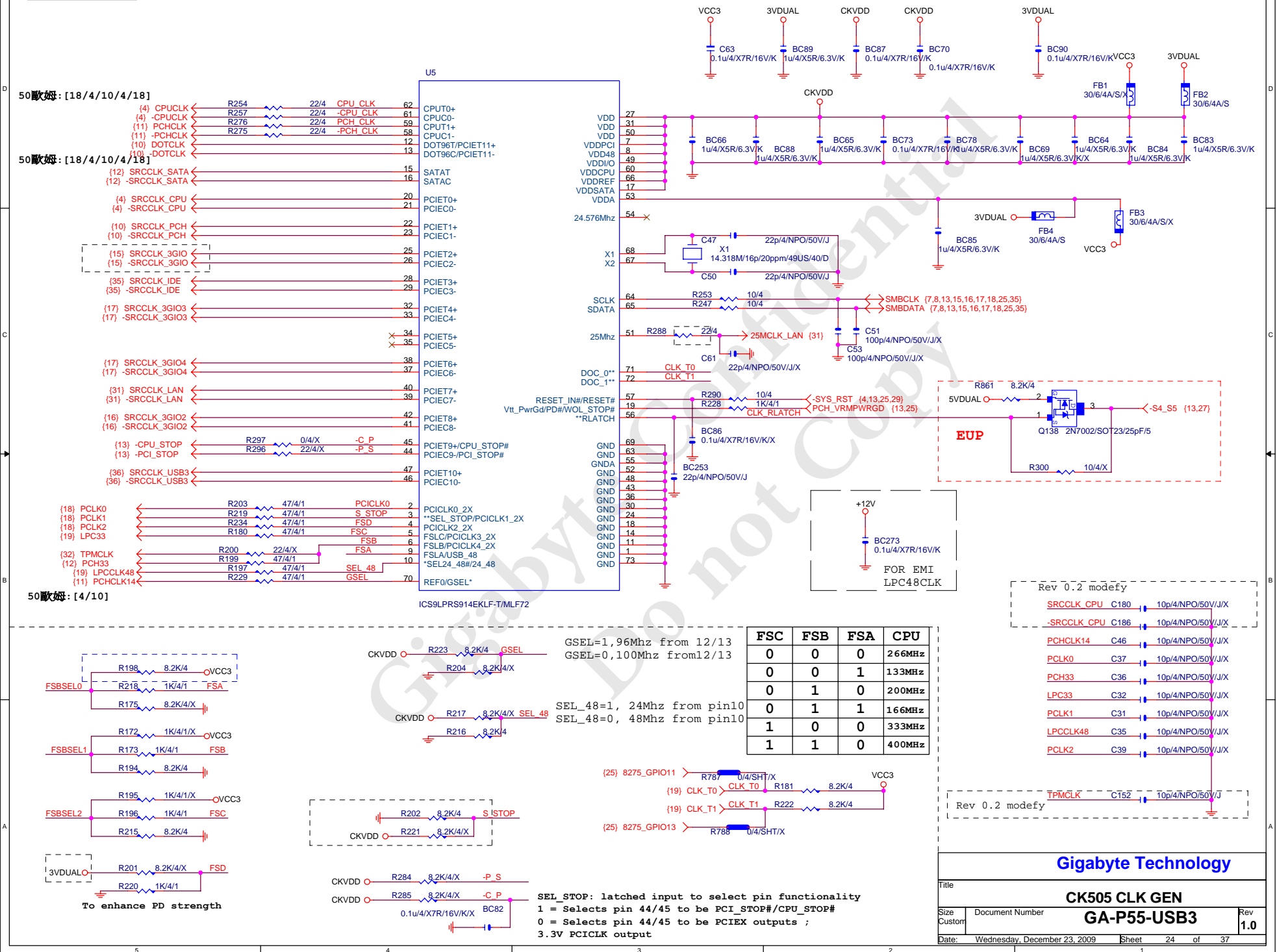
**SURR BACK**

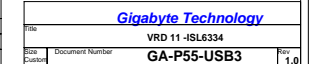


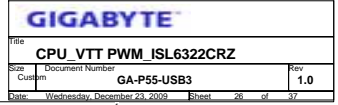
**AZALIA FRONT PANEL**

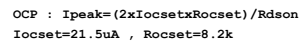


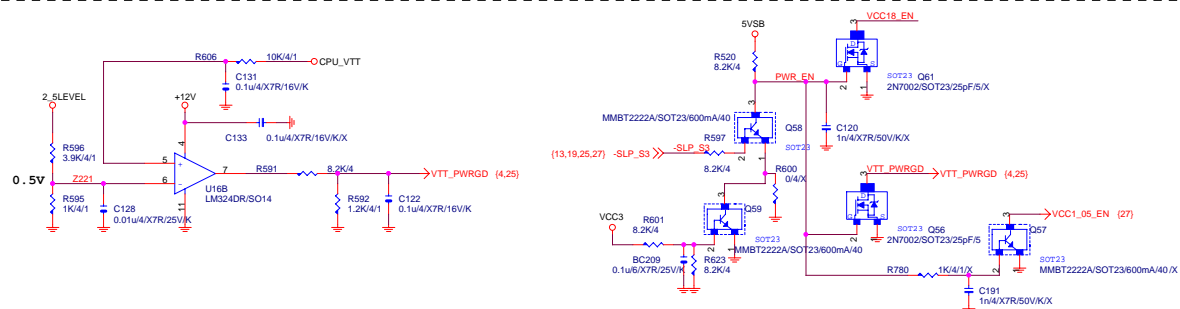
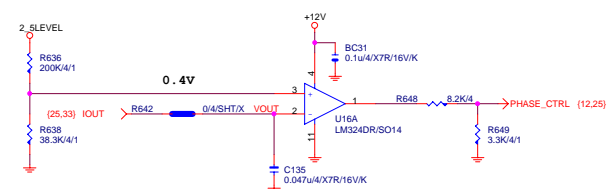
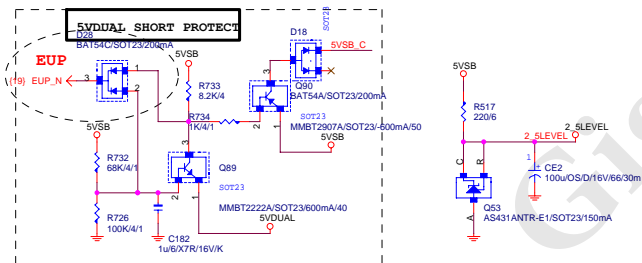
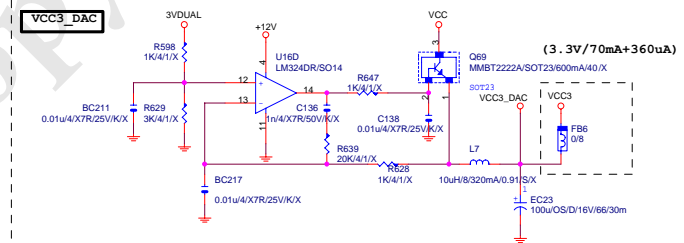
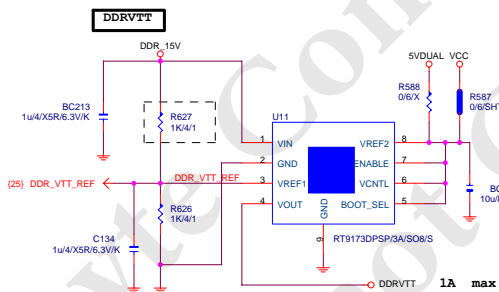
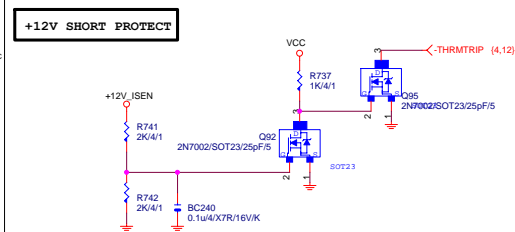
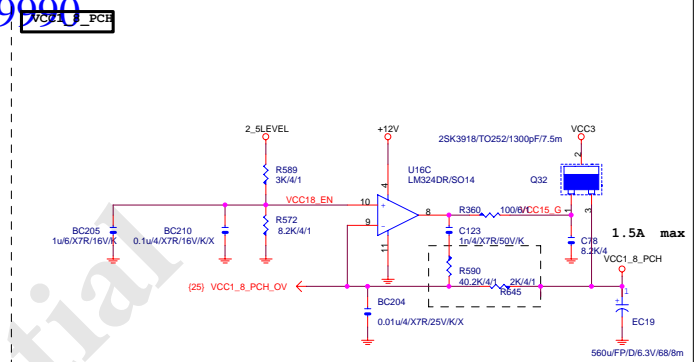
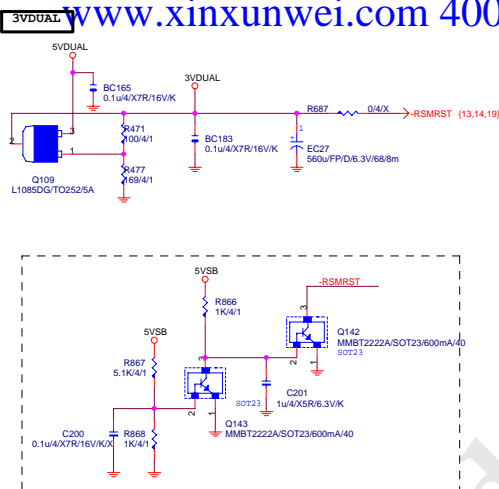
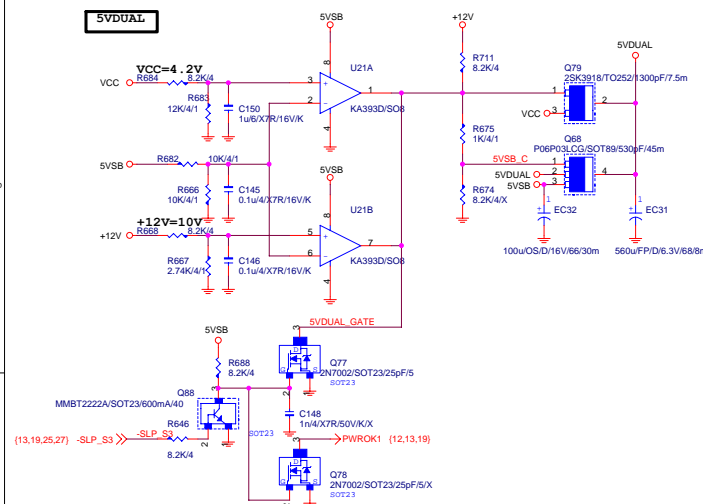




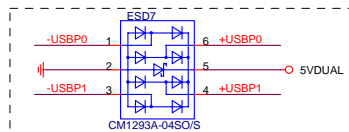
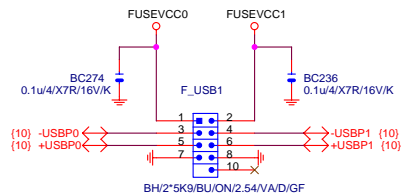






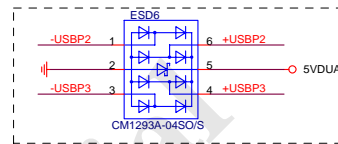
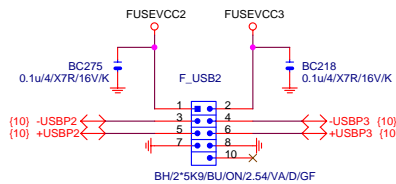


## FRONT USB1



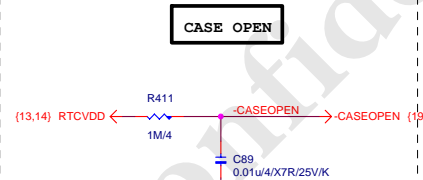
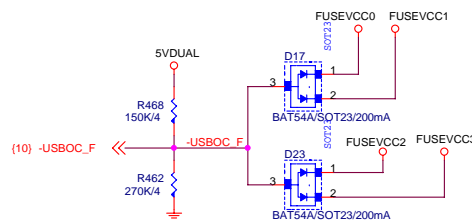
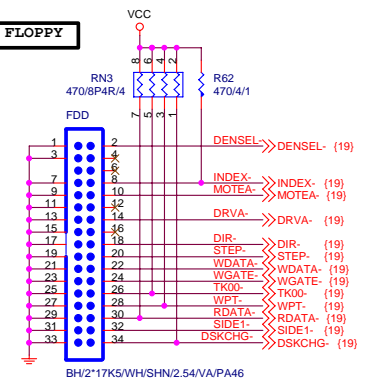
Close to connector

## FRONT USB2



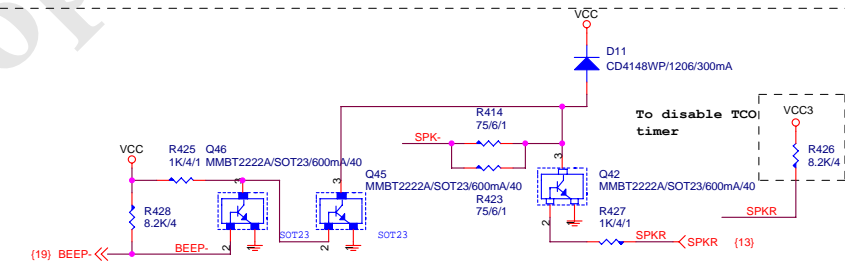
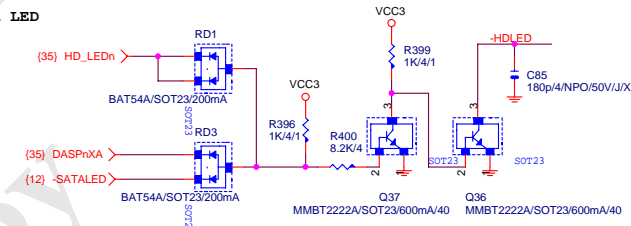
Close to connector

## FLOPPY



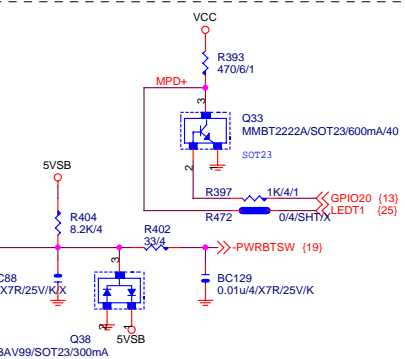
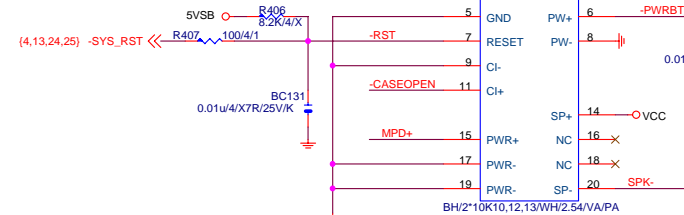
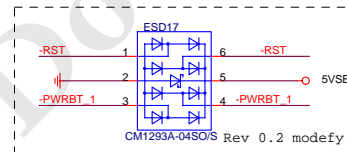
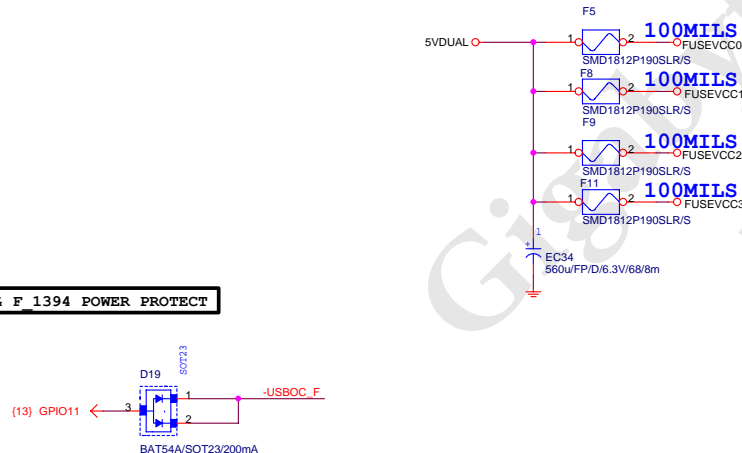
Case Open Circuits

## SATA LED



To disable TCO timer

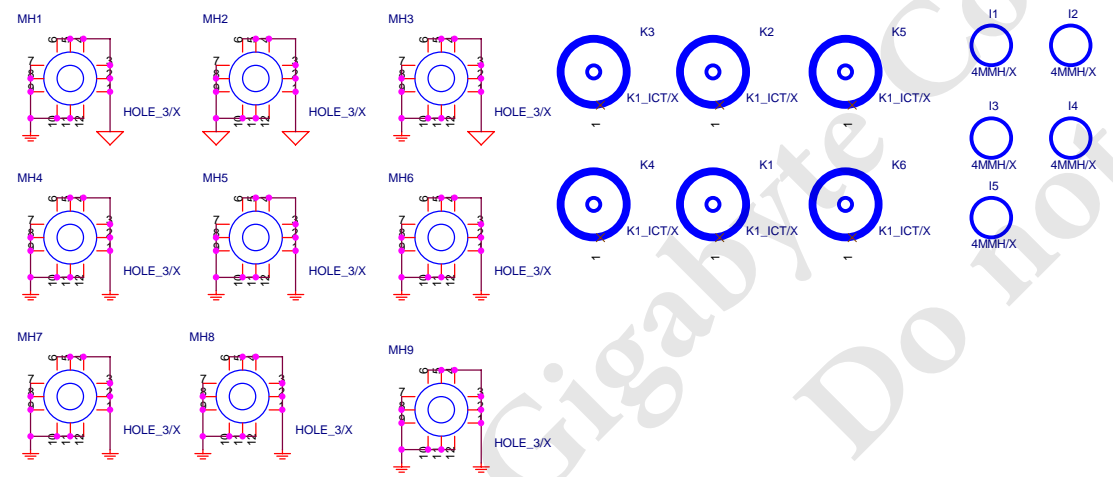
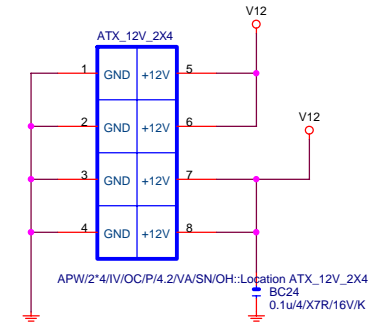
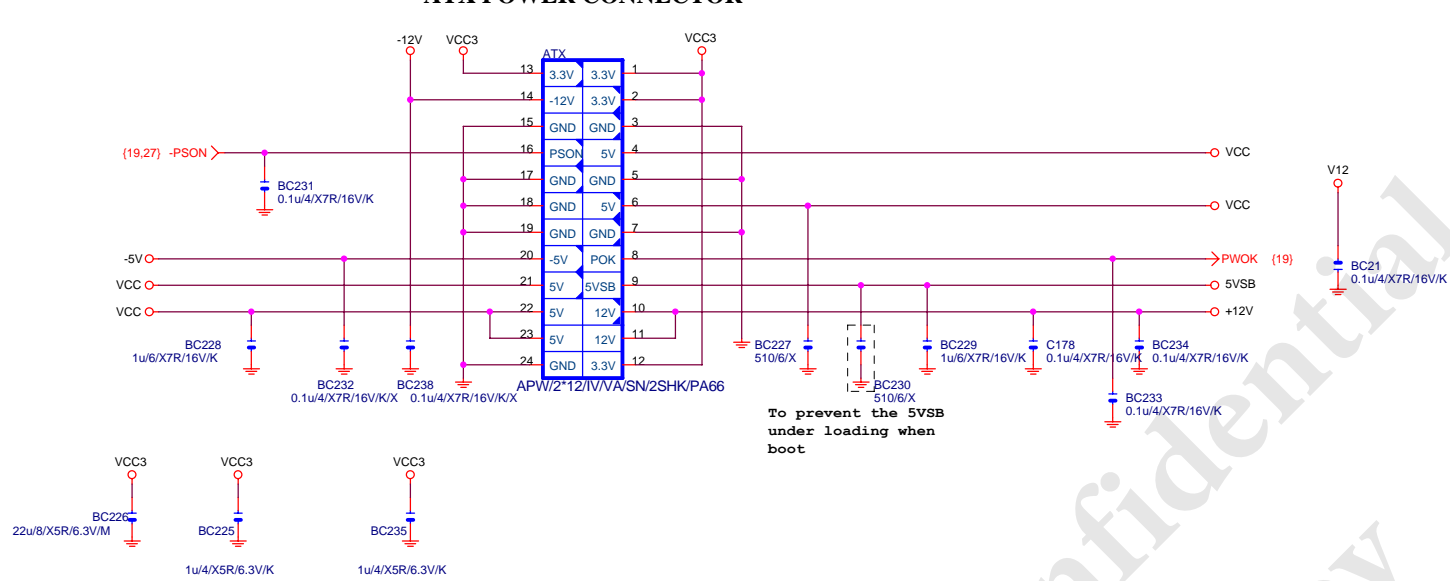
## F USB &amp; F 1394 POWER PROTECT



## Gigabyte Technology

Title		
FF,P_USB,USB PWR,FDD,BZ		
Size		
Custom	Document Number	GA-P55-USB3
Date:	Wednesday, December 23, 2009	Sheet 29 of 37
		Rev 1.0



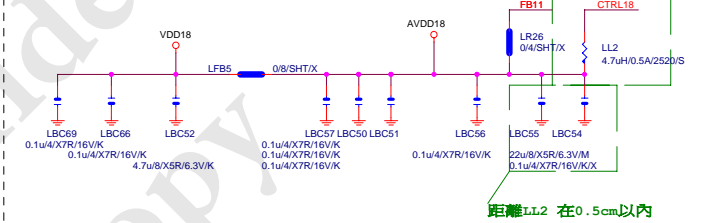
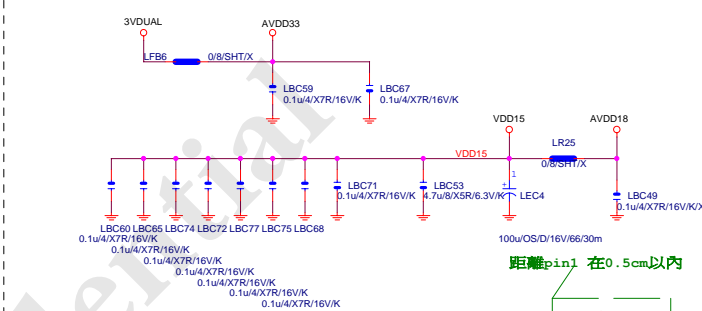
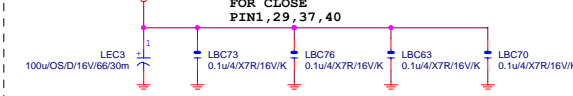
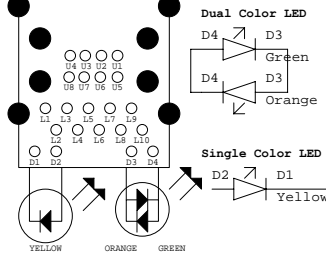


## PCIE-1G LAN

## Power domain chart

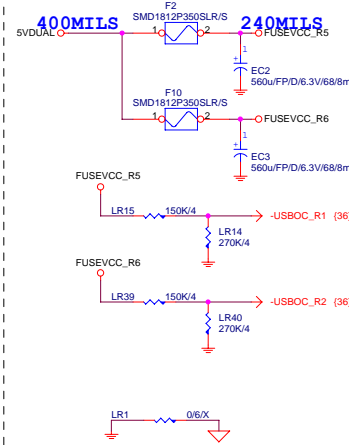
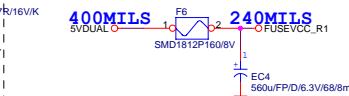
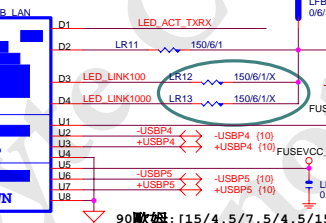
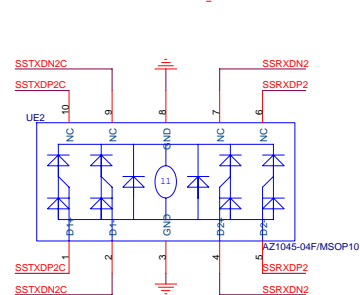
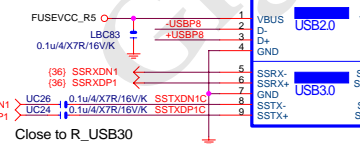
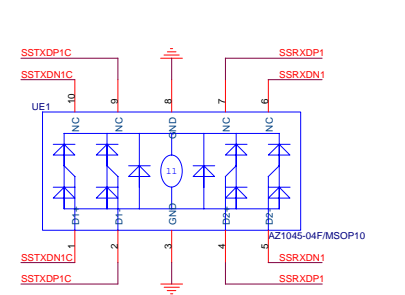
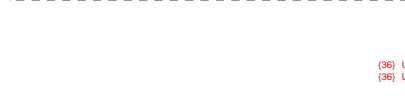
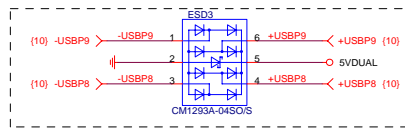
	RTL8111B/ RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
VDD15	1.5V	1.2V

for RT8111B N/C  
for RT8111C 0 ohm  
(Internal Regulator)  
for RT8111C N/C  
(external Regulator)



SEL	OE	Y+	Y-
X	H	Hi-Z	Hi-Z
L	L	M+	M-
H	L	D+	D-

## USB30\_LAN CONNECTOR



## Gigabyte Technology

REALTEK RTL8111D			
Site Custom	Document Number	Rev 1.0	
Date: Wednesday, December 23, 2009		Sheet 31	of 37

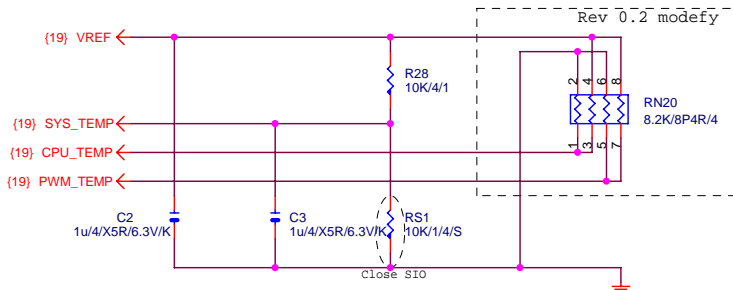


TPM I/F-SLB 9635 TT 1.2

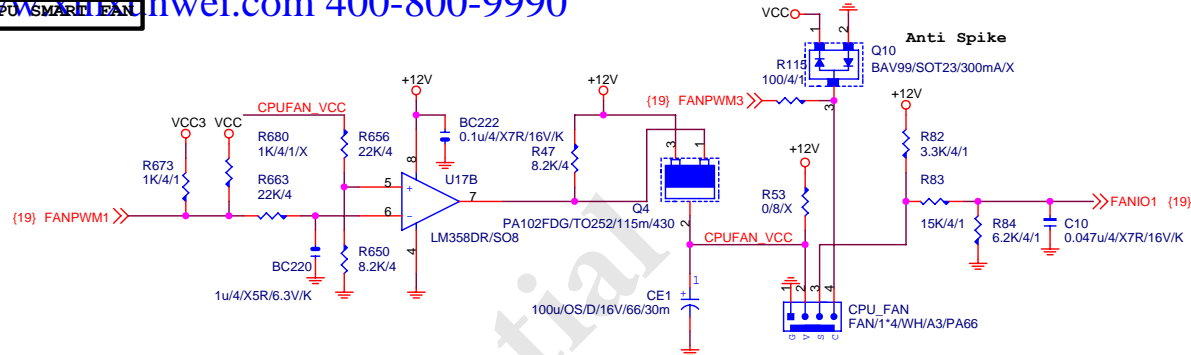
# GA-P55-USB3

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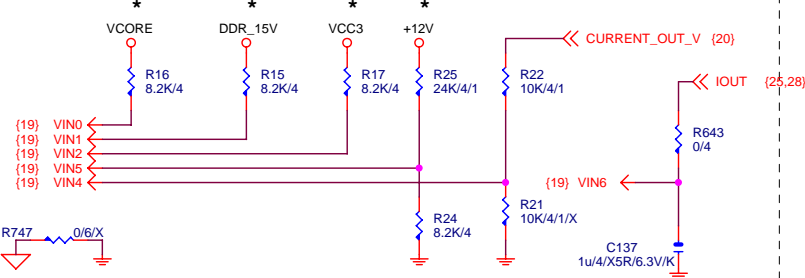
# TEMP H/W MONITOR



# CPU SMART FAN

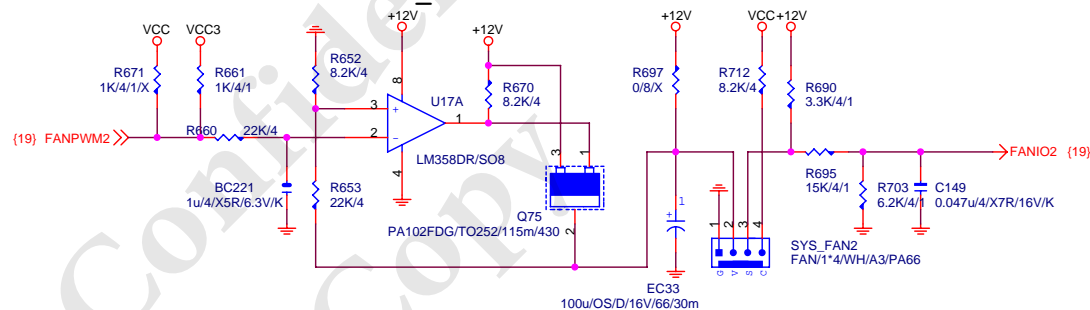


# VOLTAGE-- H/W MONITOR



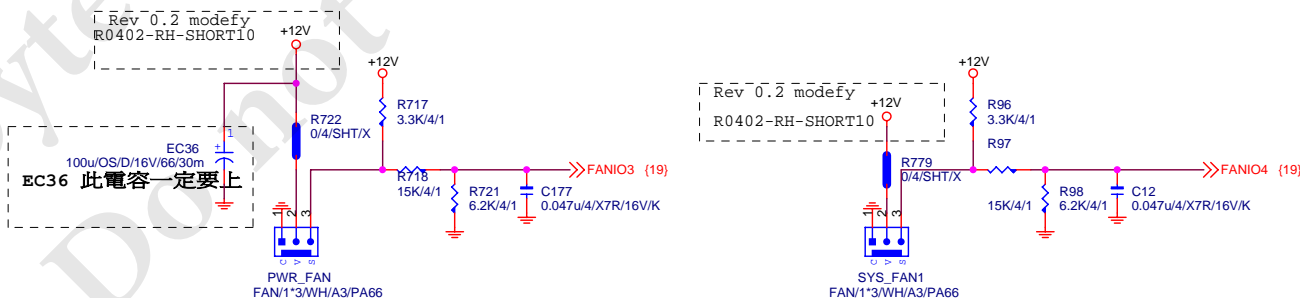
# SYS FAN2

## Linear SYS\_FAN

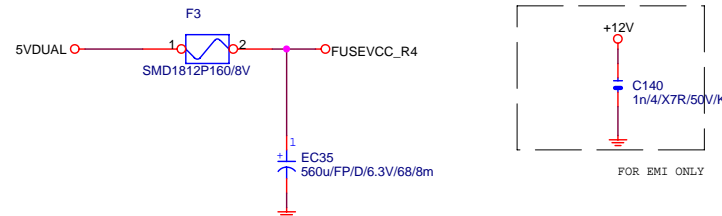
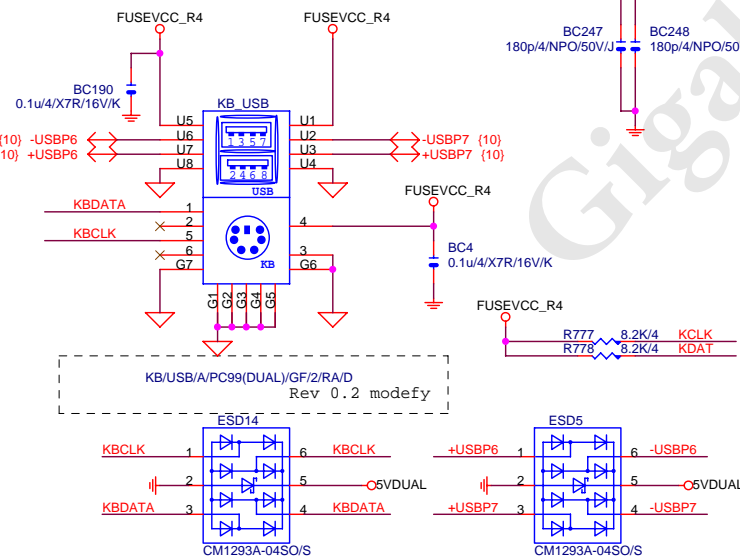


# PWR FAN

# SYS FAN1



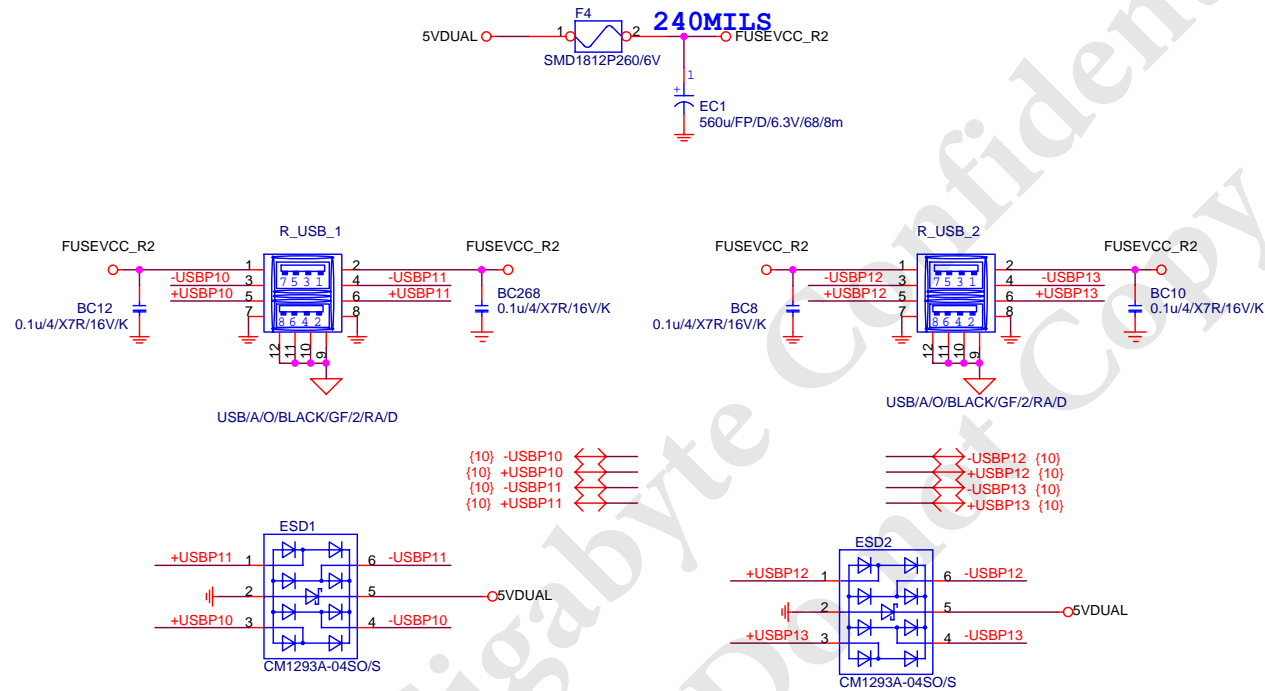
# KB/USB



Gigabyte Technology

Title			HWM,KB/MS, FAN CTRL
Size	Document Number	Rev	
Custom		1.0	
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GA-P55-USB3

**GIGABYTE™**

Title

**R\_USB**

Size

Document Number

Rev

Custom

**GA-P55-USB3****1.0**

Date:

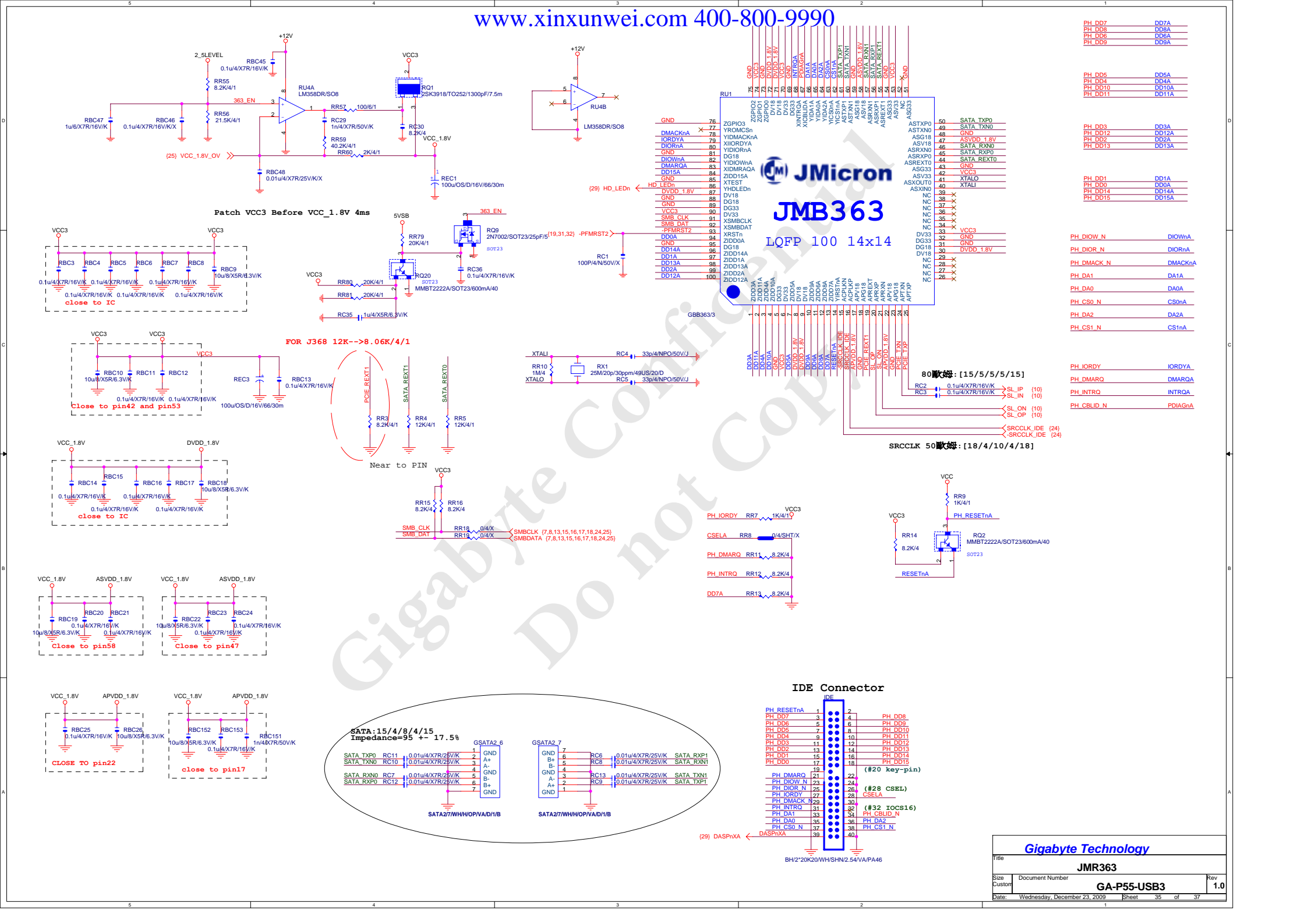
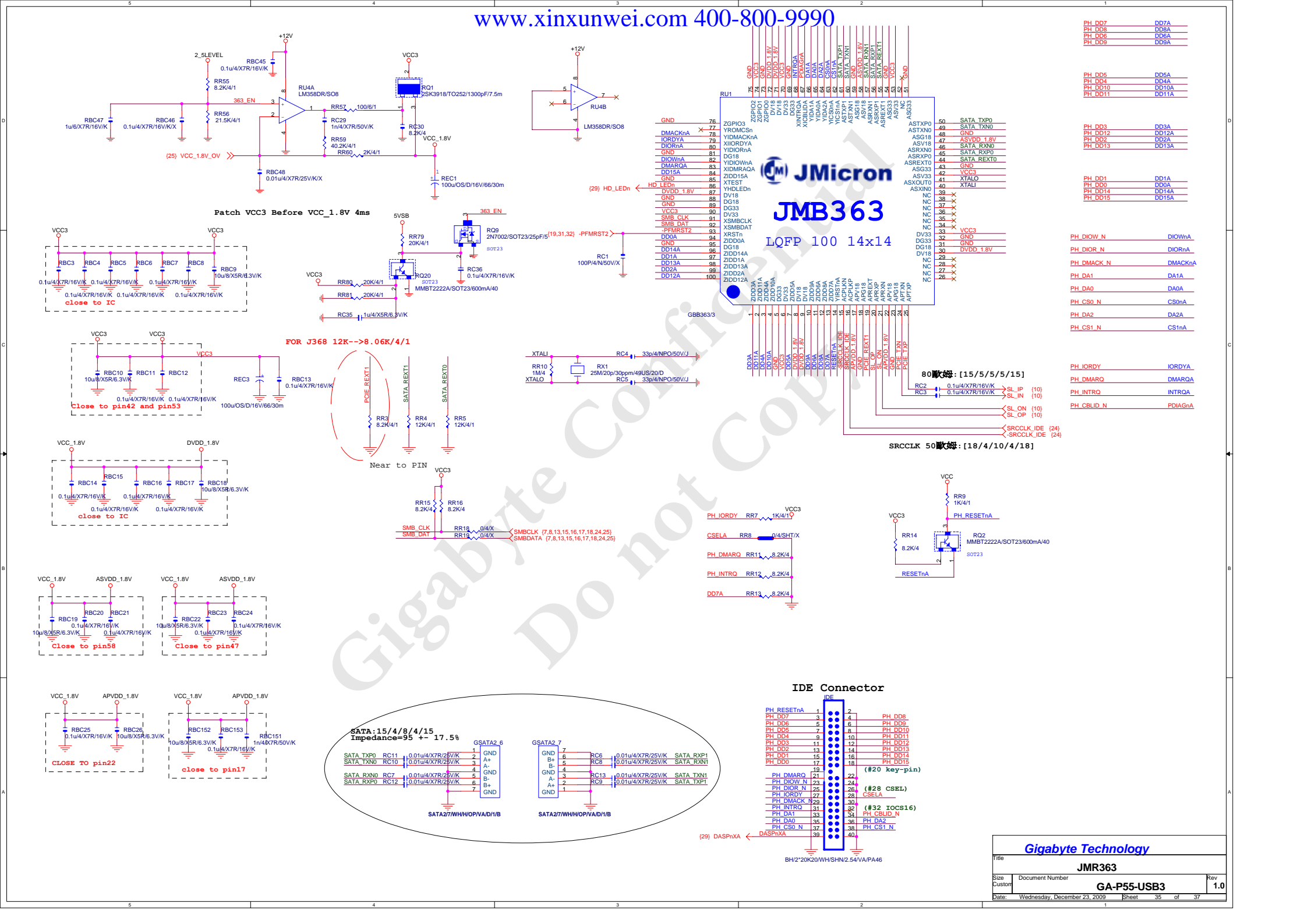
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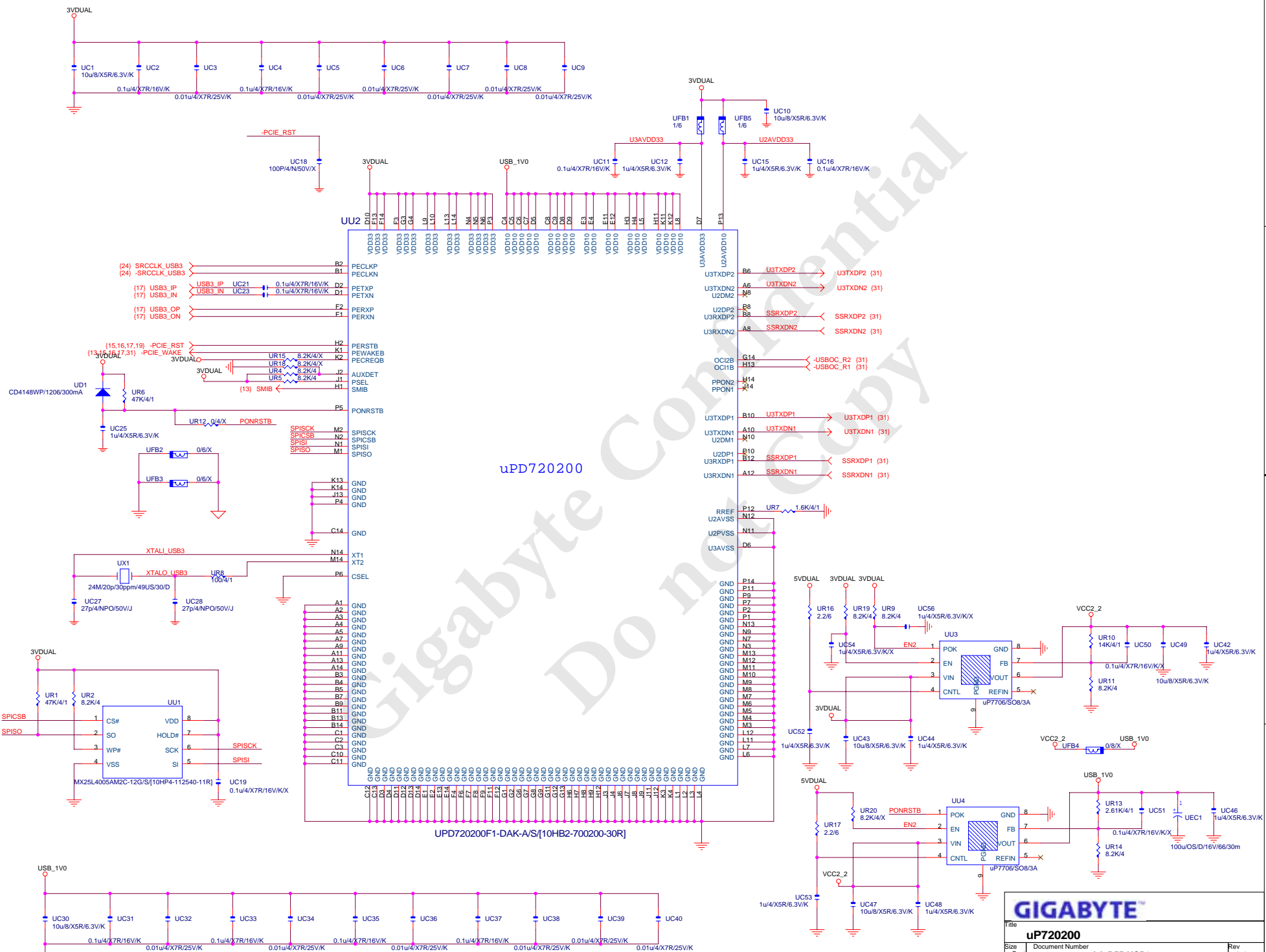
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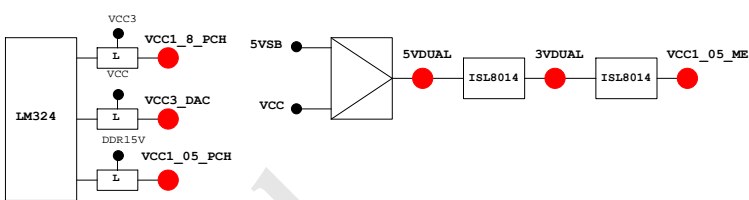


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKTOCC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_PCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A (Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A (Reverse)	P/U 8.2K 3VDUAL	

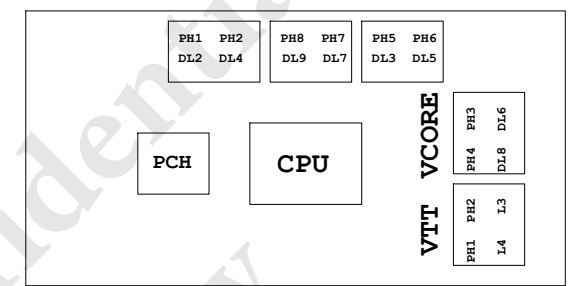
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JF7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRX1/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSS11	SB_LED1_C	
PD4/GP74/BUSS12	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSS10	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSS01	MB_ID3	
PD7/GP77/BUSS02	MB_ID4	
AED#/GP86/SMB_C_R	2X_PIN	FST_2X8
INIT#/GP85/SMB_D_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMB_C_M	DDR_LED3_C	
PWRON#/GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMB_D_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRX2/GP16	-THERM	
VIDO4/GP26/SCOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JF6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下:



BIOS超電壓對應表:

散熱模組料號:

8IBP:  
1.12SP2-01A001-Y1R/Y2R  
2.12SP2-01A001-Z1R/Z2R  
(HIBRID模組) 包材階

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

Gigabyte Technology			
File		TABLE LIST	
Size	Document Number	GA-P55-USB3	
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			1.0
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